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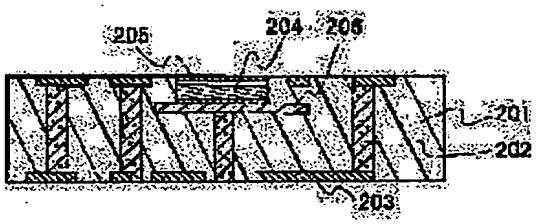
(54) SUBSTRATE INCORPORATING CHIP COMPONENT, AND MANUFACTURING METHOD OF THE SUBSTRATE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a component configuration for reducing a packaging surface and thinning the thickness of a film incorporating components when incorporating the chip component into a substrate, and manufacturing method for accurately packaging and incorporating such chip passive component as an LCR by forming a fine wiring pattern on a circuit board and at the same time forming the connection with the wiring pattern.
SOLUTION: An electrode is formed at least at either an upper or lower surface, at least one chip component is incorporated, a thickness (t) of the chip passive element 204 is smaller than length L and width W, the chip components have an external connection electrode 204 at least at one of surfaces corresponding to the upper and lower surfaces to the thickness direction, and the external connection electrode 205 is electrically connected to the wiring pattern 203 formed at an electrically insulated multilayer interconnection board 201.



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CLAIMS

[Claim(s)]

[Claim 1] It is the electric insulation wiring substrate which the electrode was formed at least in one side of a vertical side, and contained one or more chips. Thickness t of said chip passive element is die-length L and below the width of face W. And said chip The wiring substrate with a built-in chip characterized by connecting electrically the circuit pattern which has an external connection electrode at least in one side within the field corresponding to a vertical side, and was formed in it at said external connection electrode and said electric insulation multilayer-interconnection substrate to the thickness direction.

[Claim 2] The wiring substrate according to claim 1 with a built-in chip with which the active element which contains a semiconductor device in said electric insulation substrate is built in further.

[Claim 3] The wiring substrate according to claim 1 with a built-in chip said whose chip is the monolayer chip capacitor with which the electrode was formed in vertical both sides.

[Claim 4] The wiring substrate according to claim 3 with a built-in chip which the electrode formed in vertical both sides of said monolayer capacitor can consist of plurality, and can get down, and can take out two or more electrostatic capacity.

[Claim 5] The multilayer-interconnection substrate according to claim 1 with a built-in chip said whose chip is the chip passive element which consisted of multilayer structure which has the passive element formed in the interior with the conductor pattern.

[Claim 6] The wiring substrate according to claim 1, 2, or 5 with a built-in chip said whose chip is a laminating chip capacitor.

[Claim 7] The wiring substrate [equipped with the beer hall connection which penetrates said dielectric layer so that the external terminal electrode formed in the internal electrode and internal electrode which are formed in the interior of two or more dielectric layers which said laminating chip capacitor becomes from the ceramics, and said dielectric layer, the top face, or the inferior surface of tongue may connect electrically] according to claim 6 with a built-in chip.

[Claim 8] In order that it may have two or more arranged internal electrodes in said laminating chip capacitor so that it may overlap through a ceramic layer along a direction perpendicular to the inferior surface of tongue of a ceramic sintered compact, and two or more internal electrodes may take out electrostatic capacity The first external electrode which a part of the **** is exposed to the top face and inferior surface of tongue of a ceramic sintered compact, and was formed in the top face of said ceramic sintered compact, The wiring substrate according to claim 5 with a built-in chip which can be further equipped with 2nd at least one external electrode formed in the inferior surface of tongue of a ceramic sintered compact, and can take out electrostatic capacity.

[Claim 9] The wiring substrate according to claim 8 with a built-in chip which the 1st external electrode of said laminating chip capacitor and the 2nd external electrode consist of plurality, respectively, and can take out two or more electrostatic capacity.

[Claim 10] The multilayer-interconnection substrate according to claim 1 with a built-in chip the range of whose thickness of said chip passive element is 0.1mm or more 0.5mm or less.

[Claim 11] The wiring substrate according to claim 1 with a built-in chip with

which said electric insulation substrate has at least one through tube including an inorganic filler and a thermosetting resin constituent, and said through tube is filled up with the conductive paste.

[Claim 12] The multilayer-interconnection substrate according to claim 11 with a built-in chip whose rate of a thermosetting resin constituent said inorganic fillers are aluminum 2O3 and at least one filler chosen from MgO, BN, AlN, and SiO2, and the rate of the inorganic filler is 70 - 95 % of the weight, and is 5 - 30 % of the weight.

[Claim 13] The wiring substrate according to claim 1 with a built-in chip with which said electric insulation substrate becomes at least one reinforcing materials chosen from the group which consists of the textile fabrics of a glass fiber, the nonwoven fabric of a glass fiber, textile fabrics of heat-resistant organic fiber, and a nonwoven fabric of heat-resistant organic fiber, and its reinforcing materials from what sank in the thermosetting resin constituent, it has at least one through tube, and said through tube is filled up with the conductive paste.

[Claim 14] The wiring substrate according to claim 1 with a built-in chip in which said chip passive element was mounted with electroconductive glue.

[Claim 15] The wiring substrate according to claim 2, 3, or 6 with a built-in chip to which said wiring layer with a built-in chip capacitor and said semiconductor device performed decoupling, and were connected through beer or a bump in the multilayer-interconnection substrate containing said semiconductor device with a built-in chip.

[Claim 16] The wiring substrate according to claim 15 with a built-in chip which has the multilayer structure to which said wiring layer with a built-in chip capacitor and the wiring layer in which said semiconductor device was built carried out decoupling, and were connected through beer or a bump in the multilayer-interconnection substrate containing a semiconductor device with a built-in chip.

[Claim 17] The wiring substrate according to claim 15 with a built-in chip connected in the wiring substrate having a semiconductor device and a chip by building in said chip capacitor and said semiconductor device in the same layer,

and each component performing decoupling through beer or a bump.

[Claim 18] The wiring substrate according to claim 1 with a built-in chip whose thickness t of said chip passive element thickness t of said chip passive element is 5 - 90% of die-length L, and is 5 - 90% of the width of face W.

[Claim 19] Make a metal layer adhere to a carrier layer directly through stratum disjunctum, and a circuit pattern configuration is processed. The components circuit pattern formation material for an imprint which mounted the chip passive element while forming the circuit pattern for an imprint and carrying out alignment to said circuit pattern configuration for an imprint is used. It arranges so that one [at least] front face of the sheet-like base material with which the side in which said components circuit pattern was formed constitutes an electric insulation substrate may be contacted. The manufacture approach of a wiring substrate including imprinting said components circuit pattern which pastes up and embeds these, exfoliates said circuit pattern metal layer for an imprint from a carrier layer, and contains a metal layer and a chip in said sheet-like base material at least with a built-in chip.

[Claim 20] the 2nd metal layer in which (a) carrier layer consists of the 1st metal layer, and said circuit pattern for an imprint contains the metal of the same component as the 1st metal layer through stratum disjunctum on said 1st metal layer -- forming -- a three-tiered structure -- forming -- (b) -- the manufacture approach of a wiring substrate including processing only the 2nd metal layer into a circuit pattern configuration according to claim 19 with a built-in chip.

[Claim 21] (a) carrier layer consists of the 1st metal layer, and said circuit pattern for an imprint minds stratum disjunctum on said 1st metal layer. Even the depth of the arbitration of the surface section of the 2nd metal layer, stratum disjunctum, and said 1st metal layer is processed into a circuit pattern configuration. the 2nd metal layer containing the metal of the same component as the 1st metal layer -- forming -- a three-tiered structure -- forming -- (b) -- The manufacture approach of a wiring substrate including forming concave heights in the surface section of said 1st metal layer according to claim 19 with a built-in chip.

[Claim 22] (a) A carrier layer consists of the 1st metal layer, and on said 1st metal layer, make the 2nd metal layer adhere directly and process it into a circuit pattern configuration. A chip pattern is mounted forming the circuit pattern for an imprint and carrying out alignment to the (b) aforementioned circuit pattern configuration. It arranges so that one [at least] front face of the sheet-like base material with which the side in which the components circuit pattern of this was formed constitutes an electric insulation substrate may be contacted using the components circuit pattern formation material for an imprint formed including the process to form. Said circuit pattern metal layer for an imprint containing the 2nd metal layer is exfoliated from the 1st metal layer. these -- pasting up -- embedding -- (c) -- The manufacture approach of a wiring substrate also including also imprinting said components circuit pattern which contains the 2nd metal layer and components pattern in said sheet-like base material at least with a built-in chip.

[Claim 23] The manufacture approach of a wiring substrate according to claim 22 with a built-in chip that the method of making said 2nd metal layer adhere directly, and processing a circuit pattern configuration is plating.

[Claim 24] The manufacture approach of a wiring substrate according to claim 19 to 23 with a built-in chip that said chip is mounted in said circuit pattern for an imprint by using electroconductive glue.

[Claim 25] The manufacture approach of the wiring substrate with a built-in chip which carried out the laminating of the wiring substrate with a built-in chip formed by the manufacture approach according to claim 19 to 24 further by the package laminating more than the bilayer.

[Claim 26] Make a metal layer adhere to a carrier layer directly through stratum disjunctum, and a circuit pattern configuration is processed. The components circuit pattern formation material for an imprint which mounted the semiconductor device while forming the circuit pattern for an imprint and carrying out alignment to said circuit pattern configuration for an imprint is used. It arranges so that one [at least] front face of the sheet-like base material with which the metal layer

side in which said component circuit pattern was formed constitutes an electric insulation substrate may be contacted. A wiring substrate including imprinting said components circuit pattern which pastes these up, exfoliates said circuit pattern metal layer for an imprint from a carrier layer, and contains a metal layer and a semiconductor device in said sheet-like base material at least with a built-in semi-conductor, The manufacture approach of the wiring substrate with a built-in chip characterized by obtaining the chip with which said wiring substrate with a built-in chip was connected through beer or a bump, and the decoupling of each was carried out.

[Claim 27] The manufacture approach of the wiring substrate according to claim 26 with a built-in chip which prepares said wiring substrate with a built-in semi-conductor, and said substrate with a built-in chip in the condition of having hardened to the C stage (full hardening) beforehand, the wiring layer of B stage (semi-hardening) which minded beer for each substrate layer is made to intervene, carries out a laminating, and connects a semiconductor device and a chip.

[Claim 28] The components circuit pattern formation material for an imprint which mounted the semiconductor device while made the metal layer adhere to a carrier layer directly through stratum disjunctum, the circuit pattern configuration was processed, the circuit pattern for an imprint was formed and alignment was carried out to said circuit pattern configuration for an imprint, Make a metal layer adhere to a carrier layer directly through stratum disjunctum, and a circuit pattern configuration is processed. The components circuit pattern formation material for an imprint which mounted the chip while forming the circuit pattern for an imprint and carrying out alignment to said circuit pattern configuration for an imprint is used. It arranges so that the front face of table flesh-side both sides may be contacted. each of the sheet-like base material with which the side in which these component circuit patterns were formed constitutes an electric insulation substrate -- The wiring substrate with a built-in semi-conductor which imprinted said components circuit pattern which pastes up and embeds these, exfoliates

said circuit pattern metal layer for an imprint from a carrier layer, and contains a metal layer and a semiconductor device in said sheet-like base material at least, The manufacture approach of the wiring substrate with a built-in chip characterized by obtaining the chip with which said wiring substrate with a built-in chip was connected through beer or a bump, and the decoupling of each was carried out.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the wiring substrate with which the passive component which consists of a chip with which the components circuit pattern was formed was built in, and its manufacture approach using the components circuit pattern formation material for an imprint.

[0002]

[Description of the Prior Art] In recent years, the further high density of a semiconductor and advanced features are demanded with the demand of high-performance-izing of electronic equipment, a miniaturization, and RF-izing. For

this reason, the passive component itself, such as a capacitor (C), an inductor (L), and resistance (R), is miniaturized besides said semi-conductor, and the high-density thing which also has the still smaller circuit board for mounting the chip passive component with which these properties were guaranteed further is needed.

[0003] Since the inner beer hall (IVH) continuation which is an electrical connection method between the substrate layers which can connect the electric wiring between LSI and between mounting components by the minimum distance as opposed to these demands is the most possible for the formation of high density wiring of a circuit, development is furthered in every direction. Generally, as a wiring substrate of such an IVH configuration, a multilayer ceramic wiring board, the multilayer printed circuit board by the build up method, the multilayer composite wiring substrate that consists of mixture of resin and an inorganic filler are raised, for example.

[0004] Below, as said multilayer ceramic wiring board is shown below, it can be produced. First, after preparing two or more green sheets which consist of ceramic powder, an organic binder, and plasticizers, such as an alumina, establishing a beer hall in said each green sheet and filling up said beer hall with a conductive paste, circuit pattern printing is performed to this green sheet, and the laminating of said each green sheet is carried out. And said multilayer ceramic wiring board is [this layered product] producible a debinder and by calcinating. Since such a multilayer ceramic wiring board has IVH structure, it can form a very high-density circuit pattern, and is the the best for the miniaturization of electronic equipment etc.

[0005] Moreover, the printed-circuit board by said build up method which imitated the structure of this multilayer ceramic wiring board is also developed in every direction. For example, as a build up method general to JP,9-116267,A and JP,9-51168,A, after using as a core the glass-epoxy group plate currently used from the former and forming a photosensitive insulating layer in this substrate front face, the approach of preparing a beer hall by the photolithography method,

performing coppering all over this further, carrying out chemical etching of said coppering, and forming a circuit pattern is indicated.

[0006] moreover, to JP,9-326562,A, the approach of filling up with a conductive paste the beer hall processed by said photolithography method indicates like said build up method -- having -- JP,9-36551,A and JP,10-51139,A -- one front face of an insulating hard base material -- a conductor -- after forming an adhesives layer in an another side front face for a circuit, respectively, preparing a through tube in this and being filled up with a conductive paste, the multilayering approach which carries out the laminating of two or more base materials in piles is indicated.

[0007] Moreover, after patent No. 2601128, patent No. 2603053, and patent No. 2587596 prepare a through tube in aramid-epoxy prepreg by laser beam machining and are filled up with a conductive paste here, they are the approach of sandwiching further and multilayering by the prepreg which carried out the laminating of the copper foil, performed patterning and was filled up with the conductive paste by using this substrate as a core.

[0008] As mentioned above, for example, if IVH connection of the resin system printed-circuit board is made, like said multilayer ceramic wiring board, the electrical installation only between required each class is possible, and since there is no through tube in the maximum upper layer of a wiring substrate, it excels also in mounting nature more further.

[0009] However, as mentioned above, the rate that the electronic parts mounted in the front face of wiring substrates, such as a capacitor and a resistor, also in the multilayer-interconnection substrate formed into high density wiring occupy is still high, and has been a big technical problem to the miniaturization of electronic equipment. The proposal which is going to lay electronic parts underground in a wiring substrate as a solution of such a technical problem, and is going to attain high-density-assembly-ization is indicated.

[0010] For example, JP,54-38561,A which laid lead loess components underground in the bore prepared in the printed circuit board, JP,60-41480,B

which laid passive elements, such as a ceramic condenser, underground in the through tube prepared in the insulating substrate, JP,4-73992,A which laid the bypass capacitor of a semiconductor device under the hole of a printed-circuit board, JP,5-218615,A, etc. are indicated.

[0011] Moreover, after embedding an electronic-parts formation ingredient at JP,8-222656,A which was filled up with the conductive matter and the dielectric matter in the beer hall established in the ceramic wiring board, and carried out coincidence baking, and the through tube prepared in the organic system insulating substrate, JP,10-56251,A which was solidified and formed the capacitor and the resistor is indicated.

[0012] Each above-mentioned conventional indication technique can be divided roughly into two methods. That is, after one of them lays already completed lead loess components, such as a chip resistor or a chip capacitor, under the through tube prepared in the wiring substrate, it connects the electrode of this lead loess component, and the circuit pattern on a wiring substrate by electroconductive paint or soldering. Moreover, in the case of an organic system wiring substrate, other one embeds electronic-parts formation ingredients, such as a capacitor, at the through tube prepared in the wiring substrate. After considering as a desired capacitor by making it solidify, plate to the end face of the upper and lower sides, form an electrode, and a wiring substrate with built-in electronic parts is made to form. Moreover, in the case of an inorganic system wiring substrate After being filled up with a dielectric paste or a conductive paste in the beer hall established in the ceramic green sheet, the wiring substrate having a desired capacitor is formed by calcinating at an elevated temperature.

[0013] However, it is difficult to acquire large capacity by the capacitor calcinated or solidified using these through tubes. On the other hand, even when a through tube is used, and it lays underground and mounts beforehand the chip capacitor with which large capacity is secured, and present and 0603 chips of the minimum size are used, a 0.6mm bed depth surely follows and it becomes difficult to realize a thin multilayer substrate.

[0014] Moreover, although the chip with which the electrode was constituted by the side face represented by 1005 and 0603 is typical in a commercial scene and the example which built them in the substrate is already proposed by JP,11-220262,A (U.S. Pat. No. 6,038,133 specification) etc. when it sees with a chip simple substance, the thing which made structure correspond in consideration of a property and a configuration to built-in, and the gestalt which made it build in a substrate are not proposed yet. Furthermore, although a monolayer chip capacitor and a thin film multilayer capacitor are in a vertical side as a component which has an electrode when it sees with a chip simple substance, carrying out the surface mount of each of these is only assumed, but, generally connecting inter-electrode with wire bond, or connecting with a ribbon lead is used. Therefore, neither building these chips in a substrate nor the effective manufacture approach connected with a sufficient precision to a circuit pattern when it is made to reach and build was yet proposed.

[0015] Especially the thing made for the heat generated from said component to radiate heat on the other hand as the resin system printed-circuit board of the high density assembly which has IVH structure generally has low thermal conductivity and mounting of components becomes high density becomes difficult when active parts, such as a semiconductor device, are mounted or built in.

[0016] The clock frequency of CPU is set to about 1GHz, and will be conjectured that the power consumption of CPU also reaches per [100-150W] one chip with the advancement of the function in A.D. 2000. Therefore, high temperature conductivity is being required of the substrate in which components are made to build.

[0017] When a substrate is seen in this viewpoint, the multilayer composite wiring substrate is proposed by JP,9-270584,A, JP,8-125291,A, JP,8-288596,A, JP,10-173097,A, etc. in order to complement that a ceramic wiring board is comparatively expensive, that a resin system printed-circuit board has a technical problem in thermal conductivity, etc. This multilayer composite wiring substrate is

a substrate which made thermosetting resin, such as an epoxy resin, and the inorganic fillers (for example, ceramic powder etc.) which are excellent in thermal conductivity mix and compound-ize, and since it is possible to contain said inorganic filler in high concentration, it can improve the thermal conductivity of said substrate. Moreover, it is possible by choosing the class of said inorganic filler to control a dielectric constant, a coefficient of thermal expansion, etc. to arbitration.

[0018] On the other hand, when advancing high density assembly of a substrate, formation of a detailed circuit pattern and formation of LCR connected with the circuit pattern, and mounting are important. In said multilayer ceramic wiring board, formation of a circuit pattern screen-stencils a thick-film conductivity paste to a ceramic substrate, and, generally the approach of burning by baking and hardening is used. However, in this screen printing, it is said that it is difficult to mass-produce the circuit pattern which is the line breadth of 100 micrometers or less. Moreover, passive components, such as LCR, were limited to the approach of carrying out a surface mount, and it was difficult for them to make it build in a substrate. Moreover, since a baking process followed in a ceramic substrate, it was impossible to have made the chip with which the property is guaranteed and which can come to hand cheaply build in. Also in this semantics, the limitation was generated in high density assembly.

[0019] Moreover, in the usual printed-circuit board, the approach of forming a circuit pattern with a subtractive process, for example is common. Although a circuit pattern is formed in a substrate in this subtractive process by carrying out chemical etching of the copper foil with a thickness of about 18-35 micrometers, it is said that it is difficult to mass-produce the circuit pattern which is the line breadth of 75 micrometers or less also by this approach, and in order to make said circuit pattern detailed further, it is necessary to make said copper foil thin.

[0020] Moreover, since it becomes the structure which the circuit pattern projected on the substrate front face according to said subtractive process, it is hard to put solder, electroconductive glue, etc. for electrical connection on the

bump who formed in the semi-conductor, and said bump moves between circuit patterns, and there is also a possibility of short-circuiting. Moreover, there is also a possibility of becoming a failure at the time of closing by closure resin for said projected circuit pattern (for example, a next process).

[0021] Moreover, it is in the inclination for an additive process to be adopted in addition to said subtractive process, in the printed-circuit board by said build up method. This additive process is the approach of plating a circuit pattern alternatively, and can form the circuit pattern which is the line breadth of about 30 micrometers in the substrate front face in which the resist was formed. However, this approach has problems, like the adhesion reinforcement of the circuit pattern to a substrate is weak compared with said subtractive process.

[0022] Then, after forming a detailed circuit pattern beforehand and conducting pattern inspection, the approach of imprinting only the circuit pattern of an excellent article to a desired substrate is devised. For example, a U.S. Pat. No. 5,407,511 number is the approach of forming a detailed pattern in the front face of a carbon plate by printing and baking, and imprinting this to a ceramic substrate beforehand.

[0023] moreover, to JP,10-84186,A and JP,10-41611,A The approach of imprinting to prepreg the circuit pattern which consists of copper foil formed on the mold-release characteristic support plate is indicated. Similarly to JP,11-261219,A The approach of imprinting the circuit pattern which consists of copper foil through nickel phosphorus alloy stratum disjunctum on the mold-release characteristic support plate which consisted of copper foil again to JP,8-330709,A The approach which the adhesion degree in the roughening side and glossy surface of copper foil which are a circuit pattern imprints to a substrate using differing, respectively is indicated.

[0024] The circuit pattern imprinted by such replica method is embedded on a substrate front face, and since it becomes structure with the flat front face of the wiring substrate obtained, the problem by the protrusion of a circuit pattern is avoided as mentioned above. Furthermore, in the JP,10-190191,A official report,

in case a circuit pattern is embedded on a substrate front face, the effectiveness which compresses the conductive beer paste with which the through tube was made to fill up by the thickness of said circuit pattern is also indicated.

[0025]

[Problem(s) to be Solved by the Invention] However, by these approaches, each pattern formed on imprint formation material is only wiring parts, such as copper foil. Since it furthermore mounts in high density, the proposal in which LCR etc. is made to mount on imprint formation material with the gestalt of a chip is also made, but the present chip will require a quite big mounting connection area as compared with components area, if it is made to mount by an alder DARI flow etc., since the electrode is formed in the side face. In order to mount where a chip is stood so that an electrode may become perpendicular on imprint formation material, in order to prevent it, and to make it imprint and build in a substrate, various problems, such as reservation of the thick thickness more than a location gap of a chip and the die-length part of a chip, arise at the time of embedding, and limitation increases on the design of a multilayer substrate. Moreover, when mounting and carrying out imprint built-in with wire bond on imprint formation material, it will embed, after carrying out the resin seal of the field and protecting it beforehand. However, since wiring between components becomes long when it connects with wire bond, it is reported by the RF application that a property deteriorates.

[0026] Then, this invention aims at offering the manufacture approach which mounts chip passive components, such as LCR, correctly and builds them in, forming connection with a circuit pattern, forming a circuit pattern small a component-side product and detailed to the bill of materials which can do thickness with built-in components thinly, and the circuit board in building a chip in a substrate.

[0027]

[Means for Solving the Problem] In order to attain said purpose, this invention persons propose the chip passive element by which the electrode was formed in

one of the thin vertical sides of thickness, and since it can mount and they can be correctly embedded by using imprint formation material, a thin wiring substrate with a built-in chip is offered with the shortest wiring which suited the high frequency application.

[0028] Namely, the wiring substrate with a built-in chip of this invention It is the electric insulation wiring substrate which the electrode was formed at least in one side of a vertical side, and contained one or more chips. Thickness t of said chip passive element is die-length L and below the width of face W. And said chip It is characterized by connecting electrically the circuit pattern which has an external connection electrode at least in one side within the field corresponding to a vertical side, and was formed in it at said external connection electrode and said electric insulation multilayer-interconnection substrate to the thickness direction.

[0029] Next, the 1st approach of this invention makes a metal layer adhere to a carrier layer directly through stratum disjunctum, and processes a circuit pattern configuration. The components circuit pattern formation material for an imprint which mounted the chip passive element while forming the circuit pattern for an imprint and carrying out alignment to said circuit pattern configuration for an imprint is used. It arranges so that one [at least] front face of the sheet-like base material with which the side in which said components circuit pattern was formed constitutes an electric insulation substrate may be contacted. It is the manufacture approach of a wiring substrate including imprinting said components circuit pattern which pastes up and embeds these, exfoliates said circuit pattern metal layer for an imprint from a carrier layer, and contains a metal layer and a chip in said sheet-like base material at least with a built-in chip.

[0030] Next, as for the 2nd approach of this invention, (a) carrier layer consists of the 1st metal layer. On said 1st metal layer, make the 2nd metal layer adhere directly and it is processed into a circuit pattern configuration. A chip pattern is mounted forming the circuit pattern for an imprint and carrying out alignment to the (b) aforementioned circuit pattern configuration. It arranges so that one [at least] front face of the sheet-like base material with which the side in which the

components circuit pattern of this was formed constitutes an electric insulation substrate may be contacted using the components circuit pattern formation material for an imprint formed including the process to form. Said circuit pattern metal layer for an imprint containing the 2nd metal layer is exfoliated from the 1st metal layer. these -- pasting up -- embedding -- (c) -- It is the manufacture approach of a wiring substrate also including also imprinting said components circuit pattern which contains the 2nd metal layer and components pattern in said sheet-like base material at least with a built-in chip.

[0031] Next, the 3rd approach of this invention makes a metal layer adhere to a carrier layer directly through stratum disjunctum, and processes a circuit pattern configuration. The components circuit pattern formation material for an imprint which mounted the semiconductor device while forming the circuit pattern for an imprint and carrying out alignment to said circuit pattern configuration for an imprint is used. It arranges so that one [at least] front face of the sheet-like base material with which the metal layer side in which said component circuit pattern was formed constitutes an electric insulation substrate may be contacted. A wiring substrate including imprinting said components circuit pattern which pastes these up, exfoliates said circuit pattern metal layer for an imprint from a carrier layer, and contains a metal layer and a semiconductor device in said sheet-like base material at least with a built-in semi-conductor, It is the manufacture approach of the wiring substrate with a built-in chip characterized by obtaining the chip with which said wiring substrate with a built-in chip was connected through beer or a bump, and the decoupling of each was carried out.

[0032] Next, the 4th approach of this invention makes a metal layer adhere to a carrier layer directly through stratum disjunctum, and processes a circuit pattern configuration. The components circuit pattern formation material for an imprint which mounted the semiconductor device while forming the circuit pattern for an imprint and carrying out alignment to said circuit pattern configuration for an imprint, Make a metal layer adhere to a carrier layer directly through stratum disjunctum, and a circuit pattern configuration is processed. The components

circuit pattern formation material for an imprint which mounted the chip while forming the circuit pattern for an imprint and carrying out alignment to said circuit pattern configuration for an imprint is used. It arranges so that the front face of table flesh-side both sides may be contacted. each of the sheet-like base material with which the side in which these component circuit patterns were formed constitutes an electric insulation substrate -- The wiring substrate with a built-in semi-conductor which imprinted said components circuit pattern which pastes up and embeds these, exfoliates said circuit pattern metal layer for an imprint from a carrier layer, and contains a metal layer and a semiconductor device in said sheet-like base material at least, Said wiring substrate with a built-in chip is connected through beer or a bump, and each is the manufacture approach of the wiring substrate with a built-in chip characterized by obtaining the chip by which decoupling was carried out.

[0033]

[Embodiment of the Invention] It is the electric insulation multilayer-interconnection substrate which contained the chip passive element by which the electrode was formed in either even if few. this invention -- a vertical side -- Thickness t of said chip passive element is set up smaller than die-length L and width of face W. It is the multilayer-interconnection substrate with a built-in chip to which the circuit pattern which has the external connection electrode within the field corresponding to a vertical side settled in a field at least at either, and was formed at said external connection electrode and said electric insulation multilayer-interconnection substrate was connected to the thickness direction.

[0034] Since a new area accompanying mounting did not occur since the electrode was constituted by the vertical side unlike the substrate having the usual chip, and the chip with thin thickness is used for this, it can form small [of volumetric efficiency / very high], and the thin-shape-ized substrate with a built-in chip.

[0035] In the above, it is desirable that the active element which contains a semiconductor device in said electric insulation substrate is built in further.

[0036] Moreover, small-area-izing said chip passive element becomes being the monolayer chip capacitor with which the electrode was formed in vertical both sides possible very thinly. Furthermore, the capacity spec. of a monolayer chip capacitor can realize a value more exact 10 or more times than the usual laminating chip capacitor, and can demonstrate effectiveness for the application in the severe RF of a design.

[0037] Moreover, the electrode configuration formed in vertical both sides of said monolayer capacitor can consist of two or more plurality, can get down, and can take out two or more electrostatic capacity as the result.

[0038] Moreover, said chip passive element is the chip which consisted of multilayer substrates which have the passive element formed in the interior with the conductor pattern, for example, can respond to a laminating chip inductor, a laminating chip capacitor, etc., and the large inductance quality was guaranteed to be, and the substrate with a built-in chip which has large capacity can be realized.

[0039] Moreover, it is desirable to have had the beer hall connection which penetrates said dielectric layer so that the external terminal electrode formed in the internal electrode and internal electrode which are formed in the interior of two or more dielectric layers which a laminating chip capacitor becomes from the ceramics, and this dielectric layer, the top face, or the inferior surface of tongue may connect electrically. Therefore, since the distance of a terminal electrode and an interior product layer electrode serves as short structure only with an inferior-surface-of-tongue electrode as compared with the case where they are the point which can take out a connection terminal, and the conventional side-face electrode, stray capacity can be made small and the point which is easy to draw an exact capacity is mentioned as an advantage.

[0040] Moreover, in order that it may have two or more arranged internal electrodes in a laminating chip capacitor so that it may overlap through a ceramic layer along a direction perpendicular to the inferior surface of tongue of a ceramic sintered compact, and two or more internal electrodes may take out electrostatic

capacity It is exposed to the top face and inferior surface of tongue of a ceramic sintered compact, and a part of the **** can be further equipped with the first external electrode formed in the top face of said ceramic sintered compact, and 2nd at least one external electrode formed in the inferior surface of tongue of a ceramic sintered compact, and it can take out electrostatic capacity. Therefore, since a terminal electrode can be constituted in a vertical side, without using a beer hall connection, a chip capacitor is easily producible. Moreover, since the laminated structure is adopted, the substrate with a built-in chip capacitor by which can obtain a mass capacitor and thickness is not accompanied can be obtained.

[0041] Moreover, the electrode configuration formed in vertical both sides of said multilayer capacitor can consist of two or more plurality, can get down, and can take out two or more electrostatic capacity as the result.

[0042] Moreover, if the thickness of a chip passive element is 0.1mm or more, things can be carried out and the thickness which is dealt with so that a crack etc. may not be produced and which built in the chip as it is the range of 0.5mm or less on the other hand can be stopped.

[0043] Moreover, if an electric insulation substrate has at least one through tube including an inorganic filler and a thermosetting resin constituent and said through tube is filled up with the conductive paste, it excels in ** and **** and a chip can be embedded easily.

[0044] Moreover, an inorganic filler is at least one inorganic filler chosen from aluminum 2O3 and the group which consists of MgO, BN, AlN, and SiO2, the rate of the inorganic filler is 70 - 95 % of the weight, and it is desirable that the rate of a thermosetting resin constituent is 5 - 30 % of the weight. since high density is extremely filled up with the inorganic filler according to this example, if aluminum 2O3 is chosen as an inorganic filler, for example -- a general organic system resin substrate -- comparing -- high temperature -- a substrate [****] is obtained and the property of an inorganic filler can be employed efficiently.

[0045] Moreover, an insulating substrate becomes at least one reinforcing

materials chosen from the group which consists of the textile fabrics of a glass fiber, the nonwoven fabric of a glass fiber, textile fabrics of heat-resistant organic fiber, and a nonwoven fabric of heat-resistant organic fiber, and its reinforcing materials from what sank in the thermosetting resin constituent, it has at least one through tube, and said through tube may be filled up with the conductive paste.

[0046] Moreover, if a chip passive element is mounted with electroconductive glue and adopts the chip of a non-lead system ingredient, the substrate with a built-in chip of a non-lead system is completely producible.

[0047] Moreover, a wiring layer with a built-in chip capacitor and said semiconductor device perform decoupling, and minimum distance mounting with a semiconductor device and a chip capacitor is realized as it is the structure connected through beer or a bump, and the device which has the property which was [-ization / low noise] excellent can be realized. Here, decoupling means shutting up the radio noise generated in the thing of IC of operation in the high-speed circuit of IC circumference as much as possible, and making it not pass on an external printed circuit board or an external cable.

[0048] Moreover, a wiring layer with a built-in chip capacitor and the wiring layer in which said semiconductor device was built perform decoupling, implementation and the maximum volumetric-efficiency-izing of minimum distance mounting by it being the structure connected through beer or a bump with a semiconductor device and a chip capacitor are realized, and thin shape-ization of the whole substrate with a built-in laminating can be realized.

[0049] Moreover, said chip capacitor and said semiconductor device are built in in the same layer, and each component performs decoupling through beer or a bump, and the connected structure is desirable. According to this example, said chip capacitor and the built-in process of said semiconductor device can be performed to thin-shape-izing of the whole built-in substrate with which implementation and the maximum volumetric-efficiency-izing of minimum distance mounting with a semiconductor device and a chip capacitor were

realized, and a pan at coincidence, and a process can be made to simplify.

[0050] In this invention, 5 - 100% of die-length L of thickness t of said chip passive element is desirable, it is desirable, and 20 - 70% of its range is especially desirable. [further 5 - 90% of] 5 - 100% of the width of face W of thickness t of said chip passive element is desirable, it is desirable, and 20 - 70% of its range is especially desirable. [further 5 - 90% of] Die-length L of a chip passive element has the desirable range of 0.2mm - 2.3mm, and, more specifically, width of face W has the desirable range of 0.2mm - 2.5mm.

[0051] Next, according to the 1st approach of this invention, a chip can be easily mounted in a substrate.

[0052] Moreover, according to the 2nd approach of this invention, the chip connected with the silver circuit pattern can be easily mounted in a substrate, for example.

[0053] According to the example whose method of making the 2nd metal layer adhere directly and processing a circuit pattern configuration is plating, in said approach, a fine pattern is easily realizable.

[0054] Moreover, according to the example to which a chip uses and mounts electroconductive glue in said circuit pattern for an imprint, implementation of the wiring substrate with built-in components of a non-lead system is enabled.

[0055] Moreover, if a laminating is further carried out by the package laminating more than a bilayer, the laminating of the substrate with built-in components can be carried out easily.

[0056] Next, according to the 3rd approach of this invention, a laminating can be carried out, connecting electrically a substrate with a built-in semi-conductor, and the substrate of each other [easily] with a built-in chip.

[0057] Next, according to the 4th approach of this invention, since a semiconductor device and a chip can be made to build in coincidence, a production process can be simplified.

[0058] In said approach, the components built in at the laminating process which is degree process can be more firmly protected by preparing, where a wiring

substrate with a built-in semi-conductor and said substrate with a built-in chip are beforehand hardened to a C stage, making the wiring layer of B stage which minded beer for each substrate layer intervene, and carrying out a laminating.

[0059] In addition, in this invention, a substrate means the sheet-like base material before forming a circuit pattern etc., a wiring substrate means what formed the circuit pattern in said substrate, and the circuit board shows what mounted passive components, such as active parts or LCR, such as not only a circuit pattern but a semiconductor chip, in said substrate.

[0060]

[Embodiment of the Invention] (Gestalt 1 of operation) The configuration outline of an example of the substrate with a built-in chip which is the gestalt of operation of the 1st of this invention is shown in drawing 2 , comparing with the gestalt and drawing 1 by which the conventional proposal is made.

[0061] As it is the structure where the chip 104 with which the gestalt of the conventional substrate with a built-in chip was embedded as shown in drawing 1 (a), and the beer connection 102 formed in the substrate 101 and the wiring section 103 were connected with the wire bond 105 or is shown by drawing 1 (b), it is the structure where the embedded chip 104, and the beer connection 102 formed in the substrate 101 and the wiring section 103 were connected with solder 106. With the wire bond connection structure of drawing 1 (a), since a wire length becomes long, a problem arises especially in the property in a RF region. On the other hand, with the solder connection structure of drawing 1 (b), although the problem of a wire length is a little avoidable, the component-side product which a solder reflow takes becomes large to a chip, and has been evil at high density assembly.

[0062] on the other hand, with the substrate with a built-in chip which is said 1st operation gestalt, like drawing 2 The electrode is formed in either even if few. the built-in chip 204 -- a vertical side -- Thickness t of said chip passive element 204 is set up smaller than die-length L and width of face W. To the thickness direction, it has the external connection electrode 205 within the field corresponding to a

vertical side settled in a field at least at either, and becomes the configuration that said external connection electrode 205 and the circuit pattern 203 formed at said electric insulation multilayer-interconnection substrate 201 were connected.

[0063] Said chip passive element 204 can consider for example, a monolayer chip capacitor. From 0.25mm angle to 2.5mm angle order, thickness is covered according to capacity from 80 micrometers to 300 micrometers, and the dimension of a monolayer chip capacitor is very thin as compared with the usual laminating chip capacitor, and can derive exact capacity value. Therefore, it is not necessary with built-in to make thickness of a substrate especially thick, and is the the best for a multilayer substrate with a built-in high density chip.

[0064] Although what uses barium titanate as a principal component, and the thing which uses Pb system perovskite oxide as a principal component are mainly considered, the dielectric material of other systems is sufficient as the dielectric materials which constitute a monolayer chip capacitor.

[0065] What is necessary is not to be limited to this and just to use either besides Ag metallizing electrode and nickel electrode according to an application, although Au electrode is used as an electrode when thinking a RF property and high-reliability as important. In addition, when using Au electrode, TiW is desirable as a protective coat as an electrode of a substrate.

[0066] On the other hand, although the formation approach of said through tube for making beer connection between layers is suitably determined by the class of said sheet-like base material etc., carbon-dioxide-laser processing, processing with a punching machine, package processing by metal mold, etc. are raised, for example.

[0067] Although it will not be especially restricted as said conductive paste if it has conductivity, the resin containing the particle of a conductive metallic material etc. can usually be used. As said conductive metallic material, copper, silver, gold, silver palladium, etc. can be used and organic binders, such as epoxy system resin, phenol system resin, cellulose system resin, and acrylic resin, can be used as said resin, for example.

[0068] In addition, although the interlayer connection by conductive paste restoration is assumed, this operation gestalt is available at all, even if it is the connection structure by through hole plating beer.

[0069] (Gestalt 2 of operation) Below, the multilayer substrate with a built-in chip which is the gestalt of operation of the 2nd of this invention is shown at drawing 3 . The chip 304 built in the substrate 301 is a monolayer chip capacitor. In a top face Many electrodes 306 are formed in the inferior surface of tongue for 1 pole electrode 305. The external connection electrode 305 which is 1 pole electrode settled in these fields, and the circuit pattern 303 formed in said electric insulation multilayer-interconnection substrate 301 are connected. The external connection terminal 306 which is an a large number electrode, and the interlayer connection beer 302 formed in said electric insulation multilayer-interconnection substrate 301 are the configurations connected through the land wiring layer 307. The a large number electrode 306 formed in the inferior surface of tongue takes a grid-like gestalt, as shown in drawing 3 , and it is very good in many-items child structure.

[0070] Since two or more chip capacitors which change to the capacitor in which electrostatic capacity as a design value is not shown with mounting gestalten can be prepared according to such structure, the electrostatic capacity needed can be offered easily. This functions effectively especially, when the capacity change accompanying built-in arises.

[0071] (Gestalt 3 of operation) Next, the configuration outline of the multilayer substrate with a built-in chip which is the 3rd operation gestalt of this invention is shown in drawing 4 . In drawing 4 , the chip multilayer capacitor 404 equipped with the beer hall connection 402 which penetrates said dielectric layer so that the external terminal electrode formed in the internal electrode 404 and internal electrode which are formed in the interior of two or more dielectric layers 406 which a chip 404 becomes from the ceramics, and this dielectric layer, the top face, or the inferior surface of tongue may connect electrically is laid under the substrate 401. In addition, connection between layers is made by the beer hall

connection 407. therefore, since only an inferior surface of tongue electrode serve as the structure where the distance of an external terminal electrode and an interior product layer electrode be short, with the chip capacitor of this operation gestalt as compared with the case of the laminating chip capacitor with which the point which can take out a connection terminal by top face electrode), and the conventional external terminal electrode consist of side face electrodes, (embed backward can make stray capacity small and can derive an exact capacity for it.

[0072] (Gestalt 4 of operation) Next, the configuration outline of the multilayer substrate with a built-in chip which is the 4th operation gestalt of this invention is shown in drawing 5 . It has two or more internal electrodes 506 arranged in drawing 5 so that it may overlap through a ceramic layer along a direction perpendicular to the inferior surface of tongue of the ceramic sintered compact 505. Two or more internal electrodes The first external electrode 507 which a part of the **** is exposed to the top face and inferior surface of tongue of a ceramic sintered compact, and was formed in the top face of said ceramic sintered compact in order to take out electrostatic capacity, It has further 2nd at least one external electrode 508 formed in the inferior surface of tongue of a ceramic sintered compact, and it is the structure laid under the substrate 501, and the interlayer connection beer 502 and the external electrode 508 which were formed in the substrate 501 are connected through the wiring layer 504. Furthermore, the chip capacitor top double-sided electrode 507 and a wiring layer 503 connect, and are arranged.

[0073] According to this structure, since the laminated structure is adopted, mass electrostatic capacity can be taken out as a chip capacitor. Moreover, since a terminal electrode can be constituted in a vertical side, without using a beer hall connection, a chip capacitor is easily producible. Therefore, the substrate with a built-in chip capacitor by which is a mass capacitor and thickness is not accompanied can be obtained.

[0074] Moreover, although the chip capacitor is adopted also in each operation

gestalt and the example as a representative of a chip in this invention, an effective thing cannot be overemphasized even if it adopts a laminating ceramic inductor, a chip resistor, etc.

[0075] This multilayer capacitor is constituted using the ceramic sintered compact of a rectangular parallelepiped, for example, a proper dielectric ceramic like a barium titanate system ceramic can be used for it.

[0076] It is arranged so that two or more internal electrodes may overlap a ceramic sintered compact through a ceramic layer.

[0077] (Gestalt 5 of operation) Below, the multilayer substrate with a built-in chip which is the gestalt of operation of the 5th of this invention is shown at drawing 6 . The chip 604 built in the substrate 601 is a laminating chip capacitor. In order that it may have two or more arranged internal electrodes 606 like the gestalt 4 of operation so that it may overlap through a ceramic layer along a direction perpendicular to the inferior surface of tongue of the ceramic sintered compact 605, and two or more internal electrodes may take out electrostatic capacity Two or more external electrodes 607 which a part of the **** is exposed to the top face and inferior surface of tongue of a ceramic sintered compact, and were formed in the top face of said ceramic sintered compact, It has further two or more external electrodes 608 formed in the inferior surface of tongue of a ceramic sintered compact, and it is the structure laid under the substrate 601, and the interlayer connection beer 602 or the wiring layer 603 formed in the substrate 601 is connected to external two or more electrodes 607 or 608. Said two or more electrodes 607,608 take a grid-like gestalt, as shown in drawing 3 , and they are very good in many-items child structure.

[0078] (Gestalt 6 of operation) Below, the multilayer substrate with a built-in chip which is the gestalt of operation of the 6th of this invention is shown at drawing 7 . In order that drawing 7 may be equipped with two or more internal electrodes 706 arranged like the gestalt 4 of operation so that it may overlap through a ceramic layer along a direction perpendicular to the inferior surface of tongue of the ceramic sintered compact 705 and two or more internal electrodes may take out

electrostatic capacity The first external electrode 707 which a part of the **** is exposed to the top face and inferior surface of tongue of the ceramic sintered compact 705, and was formed in the top face of said ceramic sintered compact, It has further 2nd at least one external electrode 708 formed in the inferior surface of tongue of a ceramic sintered compact, and it is the structure laid under the substrate 701, and the wiring formative layer 703 and the external electrode 708 which were formed in the substrate 701 are connected and mounted with electroconductive glue. Therefore, since it is a solder free-lancer's mounting gestalt, if the chip of a non-lead system ingredient is adopted as said ceramic sintered compact 705, the substrate with a built-in chip which consisted of non-lead system ingredients completely is producible.

[0079] In addition, the chip built in is not limited to the chip capacitor of a laminated structure shown in drawing 7 R> 7 at all, a monolayer chip capacitor is sufficient as it, and a chip inductor and a chip resistor are also available for it.

[0080] (Gestalt 7 of operation) Below, the multilayer substrate with a built-in chip which is the gestalt of operation of the 7th of this invention is shown at drawing 8 . The chip capacitor 804 of the laminated structure of a vertical mold electrode is laid under the substrate 801 by drawing 8 like the operation gestalt 6. It is the structure where the connection beer 802 formed in the substrate 801 and the external connection electrode 806 of said chip capacitor 804 were connected. And since it is the structure where said built-in chip capacitor 804 and the semiconductor device 808 mounted in the surface of said substrate are carrying out decoupling, Minimum distance mounting with a semiconductor device 808 and a chip capacitor 804 is realized, and the device which has the property which was [-ization / low noise] excellent can be realized.

[0081] In addition, the chip built in may not be limited to the chip capacitor of a laminated structure shown in drawing 8 R> 8 at all, and a monolayer chip capacitor is sufficient as it.

[0082] (Gestalt 8 of operation) Below, the multilayer substrate with a built-in chip which is the gestalt of operation of the 8th of this invention is shown at drawing 9 .

The chip capacitor 904 of the laminated structure of a vertical mold electrode is laid under the substrate 901 by drawing 9 like the operation gestalt 7. The laminating of the structure where the connection beer 902 formed in the substrate 901 (a) and the external connection electrode 906 of said chip capacitor 904 were connected, and the structure where the semiconductor device 908 was built in the substrate 901 (b) is carried out. Since it is the structure where the wiring layer 904 with a built-in chip capacitor and the wiring layer 905 in which said semiconductor device was built are connected through the beer 902 between layers, and a chip capacitor 904 and a semiconductor device 908 perform decoupling, Thin shape-ization of the whole substrate with a built-in laminating with which implementation and the maximum volumetric-efficiency-izing of minimum distance mounting with a semiconductor device and a chip capacitor were realized is realizable.

[0083] In addition, the chip built in may not be limited to the chip capacitor of a laminated structure shown in drawing 9 at all, and a monolayer chip capacitor is sufficient as it.

[0084] (Gestalt 9 of operation) The multilayer substrate with a built-in chip which is the gestalt of operation of the 9th of this invention is similarly shown in drawing 10 . Although the structure where the interlayer connection beer 1002 which was laid under the substrate 1001 and formed in the substrate 1001, and the external connection electrode 1006 of said chip capacitor 1004 were connected has the same chip capacitor 1004 of the laminated structure of a vertical mold electrode like [drawing 10] the above-mentioned operation gestalt 8 A semiconductor device 1008 is built in the same in the same substrate 1001, and the wiring layer 1005 formed in said substrate 1001 is carrying out flip chip bonding. It is the structure where a chip capacitor 1004 and a semiconductor device 1008 furthermore perform decoupling through the beer 1002 between layers, and said wiring layer 1005. Since the process which builds in a chip capacitor 1004, and the process which builds in a semiconductor device 1008 can be performed to coincidence according to this structure, a process can be simplified and

implementation and the maximum volumetric-efficiency-izing of minimum distance mounting with a semiconductor device and a chip capacitor can be realized.

[0085] In addition, the chip built in may not be limited to the chip capacitor of a laminated structure shown in drawing 1010 at all, and a monolayer chip capacitor or a laminating chip inductor, and a chip resistor are sufficient as it.

[0086] As a substrate which, on the other hand, embeds said chip and semiconductor device, the following sheet-like base materials are desirable. For example, it is desirable that said sheet-like base material has at least one through tube including an inorganic filler and a thermosetting resin constituent, and said through tube is filled up with the conductive paste. Thereby, it excels in thermal conductivity and the high density real wearing wiring substrate which has the IVH structure where said circuit pattern was electrically connected by said conductive paste can be obtained easily.

[0087] Moreover, if this sheet-like base material is used, there is no need for high temperature processing in the case of production of a wiring substrate, for example, the low temperature treatment which is about 200 degrees C which is the curing temperature of thermosetting resin is enough.

[0088] It is desirable especially desirable that the rate of said inorganic filler is 70 - 95 % of the weight to said whole sheet-like base material, and the rate of said thermosetting resin constituent is 5 - 30 % of the weight, the rate of said inorganic filler is 85 - 90 % of the weight, and the rate of said thermosetting resin constituent is 10 - 15 % of the weight. Since said sheet-like base material can carry out high concentration content of said inorganic filler, it can set the coefficient of thermal expansion in a wiring substrate, thermal conductivity, a dielectric constant, etc. as arbitration with the content.

[0089] As for said inorganic filler, it is desirable that it is at least one inorganic filler chosen from aluminum 2O3 and the group which consists of MgO, BN, AlN, and SiO2. By determining the class of said inorganic filler suitably, it is possible to set thermal conductivity, thermal-expansion nature, and a dielectric constant

as desired conditions, for example, it is also possible to set up the coefficient of thermal expansion of the direction of a flat surface in said sheet-like base material to the same extent as the coefficient of thermal expansion of the semi-conductor to mount, and to give high temperature conductivity.

[0090] Also in said inorganic filler, for example, the sheet-like base material which used aluminum 2O3, BN, AlN, etc. is excellent in thermal conductivity, and the sheet-like base material using MgO is excellent in thermal conductivity, and a coefficient of thermal expansion can be enlarged. Moreover, SiO2 and when especially amorphous Si O2 is used, a coefficient of thermal expansion is small and the sheet-like base material of a low dielectric constant can be obtained lightly. In addition, the number of said inorganic fillers one, and they may use two or more kinds together.

[0091] The sheet-like base material containing said inorganic filler and thermosetting resin constituent is the following, and can be made and produced. First, the solvent for viscosity control is added to the mixture containing said inorganic filler and thermosetting resin constituent, and the slurry which is the slurry viscosity of arbitration is prepared. As said solvent for viscosity preparation, a methyl ethyl ketone, toluene, etc. can be used, for example.

[0092] And after carrying out film formation with a doctor blade method etc. on the mold releasing film prepared beforehand, using said slurry, processing at temperature lower than the curing temperature of said thermosetting resin and volatilizing said solvent for viscosity control, a sheet-like base material is producible by removing said mold releasing film.

[0093] Although said thickness when carrying out film formation is suitably determined by the presentation of said mixture, and the amount of said solvent for viscosity control to add, it is usually the range of 80-200-micrometer thickness. Moreover, although the conditions which volatilize said solvent for viscosity preparation are suitably determined by the class of said solvent for viscosity preparation, the class of said thermosetting resin, etc., they are 70-150 degrees C in temperature, and are usually for 5 - 15 minutes, for example.

[0094] It is PPS that it is an organic film containing at least one resin chosen from the group which can use an organic film, for example, usually consists of polyethylene, polyethylene phthalate, polyethylenenaphthalate, polyphenylene sulfide (PPS), polyphenylene phthalate, polyimide, and a polyamide as said mold releasing film desirable especially preferably.

[0095] Moreover, as another sheet-like base material, a thermosetting resin constituent is sunk into sheet-like reinforcing materials, it has at least one through tube, and there is a sheet-like base material with which said through tube is filled up with the conductive paste.

[0096] Although said sheet-like reinforcing materials will not be especially restricted if said thermosetting resin can be held, it is desirable that they are at least one sheet-like reinforcing materials chosen from the group which consists of the textile fabrics of a glass fiber, the nonwoven fabric of a glass fiber, textile fabrics of heat-resistant organic fiber, and a nonwoven fabric of heat-resistant organic fiber. As said heat-resistant organic fiber, for example, all aromatic polyamide (aramid resin), all aromatic polyester, polybutylene oxide, etc. are raised, and aramid resin is desirable especially.

[0097] Especially if it is thermal resistance, it will not be restricted, but [especially] since said thermosetting resin is excellent in thermal resistance, it is desirable that at least one resin chosen from the group which consists of epoxy system resin, phenol system resin and cyanate system resin or polyphenylene phthalate resin, and polyphenylene ether resin is included. Moreover, the number of said thermosetting resin any one, and it may use two or more kinds together.

[0098] Such a sheet-like base material is producible by making it dry and changing into a semi-hardening condition, for example, after said sheet-like reinforcing materials are immersed into said thermosetting resin constituent.

[0099] Said sinking in has the desirable thing of said thermosetting resin in said whole sheet-like base material comparatively performed so that it may become 30 - 60% of the weight.

[0100] In these manufacture approaches, when using the above sheet-like base

materials containing thermosetting resin, it is desirable to perform the laminating of said wiring substrate by hardening of said thermosetting resin by heating pressure treatment. According to this, the about 200-degree C low temperature treatment which is the curing temperature of said thermosetting resin is [in / the laminating process of said wiring substrate] enough.

[0101] Said sheet-like reinforcing materials may coat film top sheets, such as polyimide, LCP, and aramid, with heat-curing resin.

[0102] (Gestalt 10 of operation) Next, it is shown in drawing 12 , comparing with the manufacture approach and drawing 11 which are the gestalt of the conventional operation of the manufacture approach of the multilayer substrate with a built-in chip which is the gestalt of operation of the 10th of this invention.

[0103] As shown in drawing 11 (a) and (b), the soldering paste 1105 for chip connection is printed on the circuit pattern formation material for an imprint formed with the two-layer structure of the metal layer 1103 for wiring which are the metallic foil 1106 for mold release carriers whose components circuit pattern formation material for an imprint by which the proposal is already made, and which is an operation gestalt is the first metal layer, and the second metal layer formed on it. In addition, a chip may be connected with the circuit pattern for an imprint using electroconductive glue.

[0104] Next, like drawing 11 (c), after setting a chip 1104 to a position, the reflow furnace was passed and the chip was mounted on imprint formation material.

[0105] As shown in drawing 11 (d) - (e) after an appropriate time, it was stuck to the sheet-like base material 1101 with which interlayer connection beer 1102 was formed and which constitutes a substrate by pressure, performing alignment, and the imprint formation material in which the chip was mounted was forced, and hardening of a sheet-like base material was also performed to coincidence.

[0106] Then, as shown in drawing 11 (f), etching removes only metallic foil 1106 part for mold release carriers, and the substrate with which the chip 1104 was built in is obtained.

[0107] In this case, although solder mounting is carried out in the condition of

having put it to sleep at imprint formation material, a chip performs solder mounting in the condition of having stood, and also when embedding at a substrate, it is reported as a conventional example. However, in that case, the die-length direction of a chip was laid underground as it was corresponding to thickness in many cases, the thickness of the substrate became thick, and it was actually difficult to multilayer.

[0108] Anyway, in order to be stabilized and to make solder connection of the side-face electrode of the circuit pattern and chip of imprint formation material, a certain component-side product more than fixed is needed. Therefore, the thing of a chip for which wiring is arranged very much to near has become difficult, and had barred high density assembly.

[0109] On the other hand, by the manufacture approach of the gestalt operation of this invention 10th, even when it mounts with solder mounting or electroconductive glue as shown in drawing 12 (e) since the monolayer chip capacitor 1204 which has an electrode to vertical both sides will be mounted on the circuit pattern 1203 constituted by imprint formation material, a component-side product can be easily performed in the inside of a chip area, or an area equivalent to it.

[0110] According to these manufacture approaches, after forming a reverse pattern using a dry film resist (DFR), the detailed thing to do for circuit pattern formation is possible from forming a circuit pattern metal layer using direct writing methods, such as the pattern plating method including electroless deposition or electrolytic plating, and the sputtering method, vacuum deposition. Moreover, making it the same as that of copper foil can also constitute the metallic foil from which the metallic foil which constitutes a circuit pattern constitutes a carrier in the case of plating with the silver plating film which is a different metal. Moreover, since it is the same as that of the above-mentioned and it is also possible to reuse the metallic foil for carriers which is the 1st metal layer, low-cost-izing is possible and it excels also in the availability on industry.

[0111] Moreover, in case a monolayer chip capacitor is embedded using an

imprint formation agent, as shown in drawing 12 (f), since the circuit pattern for chip capacitor connection is imprinted to the sheet-like equipments 1201, you may carry out beforehand, but you may embed so that interlayer connection beer 1202 may connect with a chip 1204 directly depending on a circuit pattern.

[0112] Moreover, with the gestalt of this operation, the mold release carrier copper foil 1206 which constitutes imprint formation material is checking that only the mold release carrier 1206 instead of etching can be exfoliated, and the imprint of a components circuit pattern can be realized.

[0113] According to this manufacture approach, that there is little area which mounting of a chip takes, since thickness is also thin, the thickness of a layer with built-in components can be controlled to about 100-200 micrometers, and multilayering also becomes sufficiently possible.

[0114] (Gestalt 11 of operation) Below, the manufacture approach of the multilayer substrate with a built-in chip which is the gestalt of operation of the 11th of this invention is shown at drawing 13 .

[0115] Drawing 13 (a) As shown in - (c), after forming the adhesion film layer 1302 on the mold release resin film 1301, with the gestalt of this operation, the circuit pattern layer 1303 is formed first. After an appropriate time, the monolayer chip capacitor 1304 is mounted on imprint formation material like the operation gestalt 10. However, only one side is a single electrode and one side already consists of many electrodes for the monolayer chip capacitor 1304 used with this operation gestalt. With the gestalt of this operation, as shown in drawing 13 (g) - (i), after making mounting connection of a chip and the imprint circuit pattern by two or more electrode surface side, sticking by pressure and an embedding process are performed to the sheet-like equipments 1306, performing alignment. In embedding, as shown in drawing 13 (f), the circuit pattern by the side of one side has already been imprinted beforehand. After an appropriate time, the mold release carrier resin film was exfoliated manually. If resin is used for the film for mold release of imprint formation material like this operation gestalt, the flow of the chip mounted on imprint formation material etc. can be embedded, and it can

check beforehand in front.

[0116] Moreover, if the external terminal electrode of a monolayer chip capacitor is made into plurality like this operation gestalt, predetermined electrostatic capacity can be obtained easily. When electrostatic capacity changes with substrate built-in especially, adjustment is easy and especially effective.

[0117] In addition, although the monolayer chip capacitor is used, the manufacture approach of this operation gestalt is available at all, even if it is with drawing 5 , the laminating chip capacitor of a vertical electrode as shown in drawing 6 , a chip inductor, and a chip resistor.

[0118] (Gestalt 12 of operation) Below, the manufacture approach of the multilayer substrate with a built-in chip which is the gestalt of operation of the 12th of this invention is shown at drawing 14 . wiring which is the metallic foil 1406 for mold release carriers whose imprint formation material used for this operation gestalt is the first metal layer, the stratum disjunctum 1407 formed on it, and the second metal layer further formed on it as shown in drawing 14 -- public funds -- it is formed by the three-tiered structure of a group 1403.

[0119] In the components circuit pattern formation material for an imprint aforementioned [these], it is desirable that the bond strength of the 2nd metal layer which constitutes said the 1st metal layer and wiring layer is weak, for example, they are 50 or less gf/cm. In said 1st components circuit pattern formation material for an imprint, although between two-layer metal layers does not separate under processes, such as etching, plating, and rinsing, by using plating, vacuum deposition, etc., it is accepted that only the 2nd metal layer can be made to exfoliate easily on the occasion of Peel. Moreover, the chip pattern formed with solder or electroconductive glue can be made to exfoliate easily from the 1st metal layer which is a carrier.

[0120] On the other hand, although an organic layer thinner than 1 micrometer with adhesive strength, for example, the urethane system resin which is heat-curing resin, epoxy system resin, phenol resin, etc. can be used as stratum disjunctum in said components circuit pattern formation material for an imprint, it

is not restricted to this but other thermoplastics etc. may be used. However, if it becomes thicker than 1 micrometer, since detachability ability may get worse and an imprint may become difficult, 1 micrometer or less is desirable.

[0121] A deposit may be made to intervene as stratum disjunctum 1407 in order to reduce adhesive strength intentionally on the other hand. For example, it is also possible to make a metal deposit thinner than 1 micrometer, a nickel-plating layer, a nickel phosphorus alloy layer, or an aluminum deposit intervene between copper foil, and to give detachability.

[0122] In case this imprints to a substrate about the wiring section which consists of said 2nd metal layer, said 2nd metal layer tends to exfoliate from said 1st metal layer, and it becomes easy to imprint said the 2nd metal layer and components pattern to said substrate. In the case of a metal deposit, the thickness level of 1 micrometer is enough as stratum disjunctum from 100nm, and since process top cost starts the more the more it becomes thick, it is desirable that it is thinner than at least 1 micrometer.

[0123] In said components circuit pattern formation material for an imprint, although it is desirable that at least one metal chosen from the group which consists of copper, aluminum, silver, and nickel is included as for said 1st metal layer, it is desirable that copper is included especially. Although it is desirable that at least one metal chosen from the group which consists of copper, aluminum, silver, and nickel like the 1st metal layer is included as for said 2nd metal layer, it is desirable that silver is included in the case of said 1st components circuit pattern formation material for an imprint, and copper is included in the case of said 2nd or 3rd components circuit pattern formation material for an imprint. Because, a using [for the 1st metal layer]-copper case is for a thing cheap in cost, i.e., many foils which are commercial things and have predetermined thickness exist. Moreover, when using copper for the 2nd metal layer, it is because generating by plating is easy. Moreover, if the 1st metal layer and the 2nd metal layer are the same in the case of the imprint formation material in the 3rd operation gestalt, it is effective in processing being

controllable by the same etching reagent, but when a metal layer is copper, there is an advantage that the FAIN processing condition broth by etching is already developed well. In addition, although ****** [the number of said metals / one], they may use two or more kinds together.

[0124] In said 1st, 2nd, and 3rd components circuit pattern formation material for an imprint, the range of the range of the thickness of said 2nd metal layer being 1-18 micrometers is 3-12 micrometers desirable especially preferably. When said thickness was thinner than 3 micrometers and said 2nd metal layer is imprinted to a substrate, there is fear which does not show good conductivity, and when said thickness is thicker than 18 micrometers, there is a possibility that it may become difficult to form a detailed circuit pattern.

[0125] In said components circuit pattern formation material for an imprint, the range of the range of the thickness of said 1st metal layer being 4-100 micrometers is 20-70 micrometers desirable especially preferably. Since the 1st metal layer serves as the structure of the surface section being etched like a wiring layer and having irregularity as shown in this operation gestalt depending on the case while it functions as a carrier, it is desirable that it is a metal layer with sufficient thickness. Moreover, sufficient mechanical strength and thermal resistance are shown by using as a metal layer the carrier layer used for an imprint to heat distortion produced at the time of an imprint, and the stress-strain diagram of the direction of a flat surface.

[0126] Chemical etching for carrying out circuit pattern formation can specifically be performed as follows. If the basic-salt-ized 2nd copper water solution containing ammonium ion is used for etchant, when stratum disjunctum will consist for example, of a nickel phosphorus alloy layer, only the 2nd metal layer can be etched. Only stratum disjunctum can be removed if the mixed liquor of a nitric acid and hydrogen peroxide solution is used for an etching reagent after an appropriate time. It is used, when meaning so that the wiring section may not become in a crevice but may become flat after an imprint.

[0127] Moreover, the shape of toothing same to the 1st metal layer which

constitutes a carrier from 1 time of an etching process like this operation gestalt as a circuit pattern can be formed by making the same as that of the metallic foil which constitutes a carrier the metallic foil which constitutes a circuit pattern.

[0128] Moreover, it is also possible to use for the pattern formation of the way of being different as Toppan Printing using reusing the component of circuit pattern formation material for an imprint other than said 2nd metal layer after imprinting, or being processed in the shape of a circuit pattern especially in the case of the latter. For this reason, low-cost-izing is possible and it excels also in the availability on industry.

[0129] In addition, in the configuration of the components circuit pattern for an imprint aforementioned [these], said metal layer may be formed on said 2nd metal layer with electrolysis plating on the 2nd circuit pattern. If the 3rd metal layer or the metal layer for said circuit pattern formation is formed with said electrolysis plating, since a clearance does not occur between said metal layers, for example, even if it performs etching etc., an adhesive property moderate to the adhesion side of said 2nd metal layer and said 3rd metal layer is not only acquired, but it can form a good circuit pattern. On the other hand, after forming said 3rd metal layer by panel plating on the 2nd metal layer, it may mask on a circuit pattern and pattern formation may be performed. In this case, effectiveness is in scaling prevention of the 2nd metal layer after an imprint, and the improvement of pewter wettability.

[0130] In the manufacture approach of this circuit pattern for an imprint, before forming the 3rd metal layer on said 2nd metal layer, it is desirable to carry out the surface roughening process of the front face of said 2nd metal layer. It says, before forming the metal layer for circuit patterns on said 2nd metal layer, or before forming said metal layer, and forming the 2nd metal layer along with said circuit pattern on the 2nd metal layer masked in the shape of [said] a circuit pattern. Thus, if the surface roughening process of said 2nd metal layer is carried out, the adhesive property of said 2nd metal layer and said 3rd metal layer will improve.

[0131] Furthermore, in the manufacture approach of said circuit pattern for an imprint, the metal layer which changes on said 3rd metal layer with electrolysis plating may be formed. Without reducing the thickness of the metal layer of the 2nd, and 3 and 4 in any way by the chemical etching method in the manufacture approach of said circuit pattern for an imprint by choosing a stable metal component chemically to the etching reagent which corrodes the metal layer which changes with said electrolysis plating, i.e., said the 1st to 3rd metal layer, since it is processible in the shape of a circuit pattern including the surface section of said 1st metal layer, it is desirable.

[0132] as the layer which consisted of this different metal -- for example -- chemical -- stable -- low -- Ag [****] or Au deposit is desirable. Since these are the metals which cannot oxidize easily, the bump of the wiring layer plated with these, the beer beforehand formed in the substrate, for example, or a bare chip, the connectability with electroconductive glue, etc. can be stabilized more.

[0133] On the other hand, when a chip and a circuit pattern are imprinted by the surface and distance between terminals, such as an inductor, a capacitor, and a semiconductor chip, is especially approaching, the imprint formation material which earns the creeping distance and which was partially processed also from semantics to the carrier layer 1406 like this operation gestalt is desirable.

[0134] Moreover, when a wiring part is a concave configuration in this way, the mounting nature which was excellent when flip chip mounting of a semi-conductor etc. was performed is demonstrated.

[0135] (Gestalt 13 of operation) The manufacture approach of the multilayer substrate with a built-in chip which is the gestalt of operation of the 13th of this invention is shown below similarly at drawing 15 . This operation gestalt is characterized by carrying out the laminating of the layer with built-in components to the multilayer more than a bilayer.

[0136] As shown in drawing 15 (a), flip chip mounting of the semi-conductor bare chip 1510 is carried out on the imprint formation material in which the same circuit pattern 1503 as said operation gestalt was formed. 1509 is under-filling for

reinforcing mounting. Moreover, with this operation gestalt, the resistor 1511 formed in coincidence of printing was also added.

[0137] Since imprint formation can do a components pattern and a circuit pattern at low temperature 100 degrees C or less as for said circuit board, the condition of not hardening can be maintained also in the sheet using heat-curing resin, and as shown in drawing 15 (d), heat-curing contraction by the package laminating can be realized.

[0138] Therefore, in the circuit board which has the multilayer of four or more layers, it is not necessary to amend hardening contraction for each class. The circuit board of the multilayer structure which has a detailed circuit pattern and a components pattern by this is producible. However, about the wiring section and the components section which form a inner layer, it is not necessary to be a concave configuration as mentioned above, and flatness is sufficient.

[0139] Moreover, as shown in drawing 15 (d) and (e), when producing a multilayered circuit board like this operation gestalt, the laminating of the circuit board of each monolayer in which the semiconductor device produced as mentioned above or the chip was built is carried out, and it can produce by pasting up between layers. Though natural, the wiring layers 1512 and 1513 in which the circuit pattern of B stage and the beer between layers were formed like this operation gestalt can be added, and a laminating can be carried out to 5 lamellaes by package.

[0140] Moreover, since according to this structure the chip capacitor which functions as a semiconductor device and a bypass capacitor can be mounted so that it may be located very much in near, the outstanding property can be found out.

[0141] In addition, the components to build in cannot be limited to a chip and can also make the LCR various components of the shape of a semiconductor device and film further produced by printing etc. build in, as shown in this operation gestalt.

[0142] For example, when a sheet-like base material carries out the laminating of

the circuit board containing thermosetting resin, as shown in drawing 15 (d) - (e), like the above-mentioned, by heating pressure treatment, only said components circuit pattern is imprinted in the low-temperature region which does not heat-harden to said sheet-like base material, and the laminating of the circuit board of the obtained monolayer is carried out first. And adhesion immobilization of between said circuit boards is carried out by carrying out heating pressure treatment of said layered product with the curing temperature of said thermosetting resin, and hardening said thermosetting resin. If temperature of heating pressurization conditions is intentionally made into 100 degrees C or less and a circuitry layer is imprinted, since after an imprint can treat a sheet-like base material almost like prepreg, the multilayering of it by the package laminating which is not a laminating one by one will be attained.

[0143] Although especially the number of laminatings in said multilayered circuit board is not restricted, it is 4-8 layers and there are usually some which amount to 12 layers. Moreover, the thickness of said whole multilayered circuit board is usually 500-1000 micrometers.

[0144] In addition, the circuit board which constitutes the middle class other than the outermost layer of said multilayered circuit board may be not the crevice where the circuit pattern etc. was embedded on the front face but flatness, if the electrical installation structure by inner beer is taken into consideration. In order to acquire this structure intentionally, it is good to use the 1st [of the invention in this application], or 2nd components circuit pattern for an imprint. Moreover, although the circuit board of structure with said flat front face is sufficient as the outermost layer of said multilayer structure, it becomes [mounting of a semiconductor chip etc.] easier that it is the wiring substrate with which the 2nd metal layer etc. was formed in the front face in the crevice at the pars basilaris ossis occipitalis of owner Perilla frutescens (L.) Britton var. crispa (Thunb.) Decne. and is desirable.

[0145] (Gestalt 14 of operation) The manufacture approach of the multilayer substrate with a built-in chip which is the gestalt of operation of the 14th of this

invention is shown below similarly at drawing 16 . This operation gestalt is characterized by carrying out the laminating of the layer with built-in components to the multilayer more than a bilayer like the operation gestalt 13.

[0146] According to the manufacture approach of this operation gestalt, the process which builds in each semiconductor device and a chip is the same as the operation gestalt 13, but the places which harden completely the sheet-like base material which is the circuit board to a built-in process and coincidence differ. According to this manufacture approach, since it has hardened completely, the layers 1601 and 1602 with a built-in each part article will be performed in the interlayer connection of a laminating through the wiring layer 1603 of B stage which plays the role of a binder.

[0147] Therefore, in a laminating process, since the components of a semiconductor device 1610 and chip 1611 grade are protected with the hardened substrates 1601 and 1602, possibility of receiving damage can already lessen them more.

[0148] (Gestalt 15 of operation) Below, the manufacture approach of the multilayer substrate with a built-in chip which is the gestalt of operation of the 15th of this invention is shown at drawing 17 . The chip and the semiconductor device are built in the layer with same built-in components, and this operation gestalt is characterized by the structure where the chip and the semiconductor device were connected by being located very much in near.

[0149] According to the manufacture approach of this operation gestalt, the point of using imprint formation material for the process which builds in each semiconductor device and a chip is the same as said operation gestalt, but the place which builds by embedding the imprint formation material 1706 containing the imprint formation material 1710 and semiconductor device 1705 containing each chip at coincidence from vertical both sides of the sheet-like base material which is the circuit board is the description. According to this manufacture approach, the layer with a built-in each part article can realize structure where the semiconductor device 1703 was connected with the chip 1704 with short

wiring through interlayer connection beer 1708, though it is one layer.

[0150] In this case, if a chip 1704 is a bypass capacitor, a semiconductor device and decoupling, such as MPU, can be performed and the outstanding function can be demonstrated.

[0151]

[Example] Below, an example is used and this invention is explained still more concretely based on drawing.

[0152] (Example 1) Drawing 12 is the sectional view showing an example of the outline of the production process of said circuit pattern formation material for an imprint. As shown in drawing 12 (a), electrolytic copper foil with a thickness of 35 micrometers was prepared as 1st metal layer 1206. First, dissolved the copper salt raw material in the alkaline bath, the rotating drum was made to electrodeposit this so that it may become high current density, the metal layer (copper layer) was formed, this copper layer was rolled round continuously, and electrolytic copper foil was produced.

[0153] Next, as shown in drawing 12 (b), the wiring reverse pattern was formed using the dry film resist 1209. As were shown in after an appropriate time at drawing 12 (c), and the laminating of the metal layer 1203 for circuit pattern formation which consisted of silver was carried out with electrolysis plating and it was shown on the field of said 1st metal layer 1206 at drawing 12 (d) so that it may become the thickness of 9 micrometers, the circuit pattern formation material for an imprint which consists of two-layer structure was produced. The center line average of roughness height (Ra) of this front face performed the surface roughening process so that it might be set to about 4 micrometers.

[0154] Next, after using and printing soldering paste to the mounting position of a monolayer chip capacitor, it equipped with said capacitor and connection was secured at the reflow furnace.

[0155] First, the substrate 1201 which imprints a circuit pattern was prepared. This substrate 1201 prepared the sheet-like base material which consists of a composite material, established the beer hall in this, and produced it by filling up

said beer hall with the conductive paste 1207. Below, the component presentation of said sheet-like substrate 1201 is shown.

[0156] (Component presentation of the sheet-like substrate 1201)

(1) the (2) liquefied 2O3 (Showa Denko [K.K.] make AS-40: particle size of 12 micrometers):90 % of the weight epoxy resin (the Japanese Lec, Inc. make --) of aluminum Weighing capacity is carried out. EF-450:9.5-% of the weight (3) carbon black (Toyo Carbon Co., Ltd. make): -- 0.2-% of the weight (4) coupling agent (Ajinomoto Co., Inc. make and titanate system:46B): -- said each component 0.3% of the weight, so that it may become said presentation Into such mixture, as a solvent for viscosity control, the methyl-ethyl-ketone solvent was added until the slurry viscosity of said mixture was set to about 20Pa and s. And the ball of an alumina was added to this, rotation mixing was carried out on condition that rate 500rpm in the pot for 48 hours, and the slurry was prepared.

[0157] Next, the polyethylene terephthalate (PET) film with a thickness of 75 micrometers was prepared, film formation was carried out to gap about 0.7mm with the doctor blade method as a mold releasing film, using said slurry on this PET film, and the film formation sheet was produced. And by leaving this film formation sheet at the temperature of 100 degrees C for 1 hour, said methyl-ethyl-ketone solvent in said sheet was volatilized, said PET film was removed, and the sheet-like base material 1201 with a thickness of 200 micrometers was produced. Since said solvent was removed at the temperature of 100 degrees C, said epoxy resin is still the condition of not hardening, and said sheet-like base material had flexibility.

[0158] This sheet-like base material was cut into predetermined magnitude using that flexibility, and the through tube (beer hall) with a diameter of 0.15mm was prepared in the location where a pitch becomes the regular intervals which are 0.2mm - 2mm using carbon dioxide gas laser. And this through tube was filled up with the conductive paste 1207 for beer hall restoration with screen printing, and said substrate was produced. Said conductive paste 1207 prepared the following ingredients so that it might become the following presentations, and it used what

was kneaded with 3 rolls.

[0159] (Conductive paste 1202)

(1) globular form copper grain child (Mitsui Mining and Smelting [Co., Ltd.] make: particle size of 2 micrometers): -- (2) 85-% of the weight bisphenol A mold epoxy resin (oil-ized shell epoxy company make --) 828:3 % of the weight guru [(3)] SHIJIRU ester system epoxy resin [of Epicoat] (Tohto Kasei Co., Ltd. make, YD-171): -- 9-% of the weight amine-adduct [(4)] curing agent (Ajinomoto Co., Inc. make, MY-24): -- next, 3% of the weight, as shown in drawing 12 (g) It has arranged so that the chip pattern side of said components circuit pattern formation material for an imprint may touch both sides of said substrate 1201, and heating pressure treatment was carried out for 5 minutes by the press temperature of 120 degrees C, and the pressure of 10kg/cm2 using the heat press. In addition, when making it the structure inserted with a vertical electrode surface about a capacitor 1204, imprint formation of the electrode pattern 1207 may be beforehand carried out on a substrate 1201.

[0160] As the epoxy resin in said substrate 1201 (epoxy resin under said sheet-like base material and conductive paste 1202) carried out melting softening and it was shown in drawing 1212 (g) by this heating pressure treatment, said chip pattern 1204 and circuit pattern 1203 were buried into said substrate 1201. And said epoxy resin was stiffened by raising whenever [stoving temperature] further and processing it for 60 minutes at the temperature of 175 degrees C.

[0161] Thereby, the elegance pattern all pasted up firmly with said sheet-like base material, and said conductive paste 1202 and each part article pattern connected electrically (inner beer connection), and it pasted up firmly.

[0162] The substrate with a built-in chip capacitor as shows the 1st metal layer 1206 which is said carrier layer to drawing 12 (h) by exfoliating was obtained from the laminating process shown in such drawing 12 (g).

[0163] The circuit board of design ****** exact [the mounting position of a chip] and strict was able to be formed easily. According to the manufacture approach using the imprint formation material containing the chip capacitor of this example,

the junction of wiring to a chip, interlayer connection beer 1202, and a circuit pattern 1203 is good, and functioned good. Moreover, even if it performed the capacitor elevated-temperature load reliability trial (125 degrees C, 50 V or 1000 hours), there is no degradation of insulation resistance in the dielectric layer of a capacitor 1204, and the insulation resistance of 106ohms or more has been secured.

[0164] As for this wiring substrate, the flat mounting front face was formed after the imprint and the hot press process. In this example, a gold plate layer may be formed on the wiring layer 1203 of this circuit board.

[0165] The thickness of a substrate layer with built-in components had realized built-in of a chip with the gestalt which is not comparatively so thick as 200 micrometers as for this circuit board, and the curvature of a substrate, a crack, and distortion were not generated.

[0166] In addition, in this example, although alumina powder is used for the inorganic filler of a substrate, oxidation silicon powder may be used. In that case, similarly, as compared with the resin substrate of the usual FR-4 grade, high temperature conductivity is maintained and was able to find out the description of the low dielectric constant 3.5.

[0167] Moreover, although carrier copper foil is used for imprint formation material, this example is available at all, even if it uses the imprint formation material which uses a resin film as a carrier.

[0168] (Example 2) Drawing 17 (a) - (d) is the sectional view showing an example of the outline of the production process of said circuit pattern formation material for an imprint which mounts a chip.

[0169] As shown in drawing 17 (a), electrolytic copper foil with a thickness of 35 micrometers was prepared as 1st metal layer 1701. Specifically the copper salt raw material was dissolved in the alkaline bath, the rotating drum was made to electrodeposit this so that it may become high current density, the metal layer (copper layer) was produced, this copper layer was rolled round continuously, and electrolytic copper foil was produced.

[0170] Next, as shown in drawing 17 (b), on the field of said 1st metal layer 1701, the thin deposit which consisted of nickel phosphorus alloys is formed, and stratum disjunctum 1702 is formed. As a metal layer 1703 for circuit pattern formation, the laminating of the same electrolytic copper foil as said 1st metal layer 1701 was carried out with electrolysis plating so that it might become the thickness of 9 micrometers, and the layered product which consists of a three-tiered structure was produced.

[0171] The center line average of roughness height (Ra) of this front face performed the surface roughening process so that it might be set to about 4 micrometers. In addition, said surface roughening process was performed by depositing a copper detailed grain in said electrolytic copper foil.

[0172] Next, it etched by the chemical etching method (it dips in a ferric chloride water solution), and patterning was performed in the surface section of the 2nd metal layer 1703 which is the circuit pattern of arbitration, and the 1st metal layer 1701.

[0173] After an appropriate time, the mask part was removed by the remover, and the circuit pattern formation material for an imprint shown in drawing 14 (d) was obtained. Since the 1st metal layer and the 2nd metal layer consist of same copper, the wiring layer of heights can be partially formed not only in the 2nd metal layer but in the 1st metal layer by one chemical etching. The description on structure is in the place processed in part to the 1st metal layer which is a carrier layer. In addition, in this example, although the nickel-plating layer is used for stratum disjunctum, even if it forms an organic layer etc., the imprint formation material which has the same structure can be obtained, for example.

[0174] In the pattern formation material of only said wiring for an imprint produced in this phase, even if the adhesive strength itself excelled [adhesive property / through the stratum disjunctum of said 1st metal layer 1701 and metal layer 1703 for circuit pattern formation] in chemical resistance that it was weak and it performed etching processing in the whole metal layer of this three-tiered structure, the circuit pattern has been formed satisfactory, without exfoliating. On

the other hand, the bond strength of said 1st metal layer 1701 and the 2nd metal layer 1703 is 40 g/cm, and was excellent in detachability.

[0175] Next, the laminating ceramic chip capacitor 1704 which has two or more vertical electrodes was connected to the interior using electroconductive glue. Since the chip multilayer capacitor 1704 of this structure had an external connection terminal in a vertical side, it was able to be easily mounted on imprint formation material.

[0176] It pushed heating 150 degrees C to sheet equipments performing the interlayer connection beer 1708 and alignment which are formed in the substrate, as similarly a semiconductor device 1705 also performs flip chip mounting on imprint formation material and shows it to drawing 17 (d). The sheet base material used for this example is the same as that of an example 1, and its same is said of the press conditions for embedding.

[0177] Although the point of using imprint formation material for the process which builds in a chip is the same as said example, the place which builds by embedding the imprint formation material 1706 containing the imprint formation material and semiconductor device 1705 containing each chip at coincidence from vertical both sides of the sheet-like base material which is the circuit board is the description.

[0178] According to this manufacture approach, the layer with a built-in each part article was able to realize structure where the semiconductor device 1705 was connected with the chip 1704 with short wiring through interlayer connection beer 1708, though it was one layer.

[0179] Consequently, the chip 1704 which is a bypass capacitor was able to perform the MPU semiconductor device 1703 and decoupling, and was able to demonstrate the outstanding function in a RF.

[0180] Moreover, as a result of imprinting the 2nd metal layer 1703 to the sheet-like base material 1707 which constitutes the circuit board, the adhesion side through the stratum disjunctum of said 1st metal layer 1701 and the 2nd metal layer 1703 exfoliated easily, and was able to imprint only said 2nd metal layer

1703 to said substrate.

[0181] The crevice corresponding to the depth by which said 1st metal layer 1701 was etched into this wiring substrate 1707 was formed, and the components pattern which includes said all wiring in the pars basilaris ossis occipitalis of said crevice was formed. Therefore, when the flip chip of the semi-conductor bare chip of further others was carried out to the surface in which the wiring layer of this crevice was formed, the outstanding mounting nature and dependability were able to be acquired.

[0182] The circuit board of design ****** exact [the mounting position of each chip] and strict was able to be formed by the package imprint. According to the imprint formation material of this example, the bump of a semiconductor chip and junction of wiring are good, and the capacitor mounted so that it might function as a bypass capacitor of a semiconductor chip also functioned good. Moreover, even if it performed the capacitor elevated-temperature load reliability trial (125 degrees C, 50 V or 1000 hours), there is no degradation of insulation resistance in the dielectric layer of a capacitor, and the insulation resistance of 106ohms or more has been secured.

[0183]

[Effect of the Invention] As mentioned above, since add the substrate with a built-in chip of this invention to formation of a detailed circuit pattern, it mounts and forms chips, such as LCR, with solder or electroconductive glue, imprints by putting them in block and is built-in-ized, it can be easily mounted correctly on a substrate. Moreover, since it has an electrode in being [which can be efficiently employed even after building in the chip property that strict property spec. was obtained by constituting the chip suitable for built-in] a point, that thickness is not bulky since chip thickness is thin, and a vertical side even if built, mounting is easy and can also make a component-side product unnecessary.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (a) and (b) are the sectional view showing the configuration outline of the substrate with a built-in chip in the gestalt of the conventional operation.
[Drawing 2] The sectional view showing the configuration outline of the substrate with built-in components in the gestalt of operation of the 1st of this invention
[Drawing 3] The sectional view showing the configuration outline of the substrate with built-in components in the gestalt of operation of the 2nd of this invention
[Drawing 4] The sectional view showing the configuration outline of the substrate with built-in components in the gestalt of operation of the 3rd of this invention
[Drawing 5] The sectional view showing the configuration outline of the substrate with built-in components in the gestalt of operation of the 4th of this invention
[Drawing 6] The sectional view showing the configuration outline of the substrate with built-in components in the gestalt of operation of the 5th of this invention
[Drawing 7] The sectional view showing the configuration outline of the substrate with built-in components in the gestalt of operation of the 6th of this invention
[Drawing 8] The sectional view showing the configuration outline of the substrate with built-in components in the gestalt of operation of the 7th of this invention
[Drawing 9] The sectional view showing the configuration outline of the substrate with built-in components in the gestalt of operation of the 8th of this invention

[Drawing 10] The sectional view showing the configuration outline of the substrate with built-in components in the gestalt of operation of the 9th of this invention

[Drawing 11] (a) - (f) is the sectional view showing the outline of the production process of each class of the multilayered circuit board formed using the conventional components circuit pattern formation material for an imprint.

[Drawing 12] (a) - (i) is the sectional view showing the outline of the production process of the substrate with a built-in chip formed using the chip circuit pattern formation material for an imprint and it in the gestalt and example 1 of operation of the 10th of this invention.

[Drawing 13] (a) - (i) is the sectional view showing the outline of the production process of the substrate with a built-in chip formed using the components circuit pattern formation material for an imprint and it in the gestalt of operation of the 11th of this invention.

[Drawing 14] (a) - (i) is the sectional view showing the outline of the production process of the substrate with a built-in chip formed using the components circuit pattern formation material for an imprint and it in the gestalt of operation of the 12th of this invention.

[Drawing 15] (a) - (e) is the sectional view showing the outline and the laminating approach of a production process of a substrate with a built-in chip in the gestalt of operation of the 13th of this invention. [of each class]

[Drawing 16] (a) - (b) is the sectional view showing the laminating approach of each class of the substrate with a built-in chip in the gestalt of operation of the 14th of this invention.

[Drawing 17] (a) - (h) is the sectional view showing the outline of the production process of the substrate with a built-in chip formed using the components circuit pattern formation material for an imprint and it in the gestalt of operation of the 15th of this invention, and the example 2 of this invention.

[Description of Notations]

1106, 1206, 1301, 1406, 1504, 1701 1st metal layer which constitutes a carrier

1208, 1302, 1407 Stratum disjunctum

103, 203, 303, 403, 503, 603, 703, 803, 903, 1003, 1103, 1203, 1303, 1403, 1503, 1612, 1703 2nd metal layer which forms a circuit pattern

101, 201, 301, 401, 501, 601, 701, 801, 901, 1001, 1101, 1201, 1306, 1401, 1501, 1605, 1706 Sheet-like base material

102, 202, 302, 402, 502, 602, 702, 802, 902, 1002, 1102, 1202, 1307, 1402, 1502, a 1708 conductivity paste

104 1104 The usual chip

204, 304, 1204, 1304, 1505, 1617 Monolayer chip capacitor

1404 Multilayer Capacitor Which Has Interlayer Connection Beer

407 Interlayer Connection Beer

404 Inner Layer Laminating Electrode (the Direction of Flat Surface)

403 External Connection Terminal

1704 Multilayer Capacitor Which Has Vertical Laminating Internal Electrode

506 Inner Layer Laminating Electrode (Lengthwise Direction)

305, 306, 403, 507, 508, 605, 608, 707, 1205 External connection terminal electrode

206, 504, 608, 707, 906, 1006, 1207 Wiring layer which connects a built-in chip and interlayer connection beer

1510, 1610, 1705 Semiconductor chip

1509 1609 Under-filling

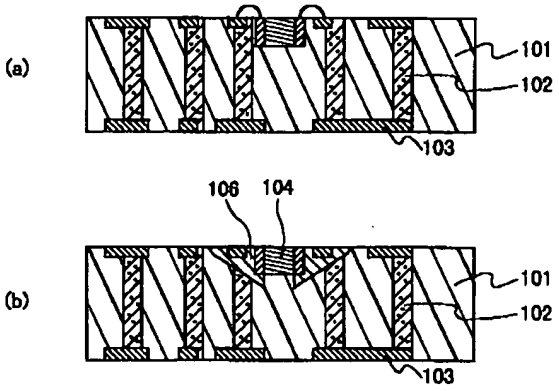
[Translation done.]

2.**** shows the word which can not be translated.

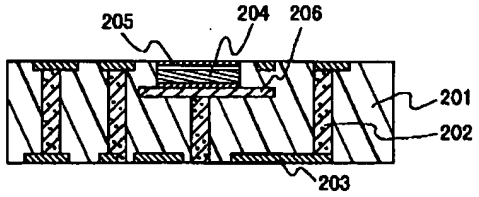
3.In the drawings, any words are not translated.

DRAWINGS

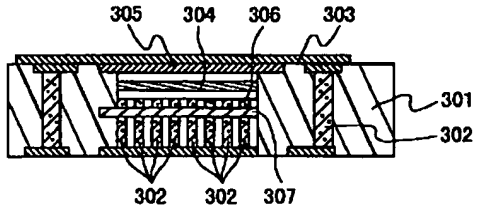
[Drawing 1]



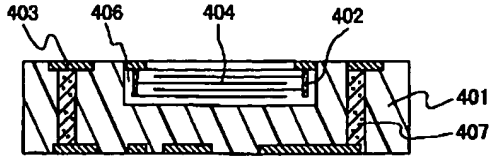
[Drawing 2]



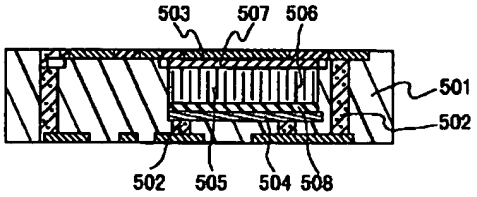
[Drawing 3]



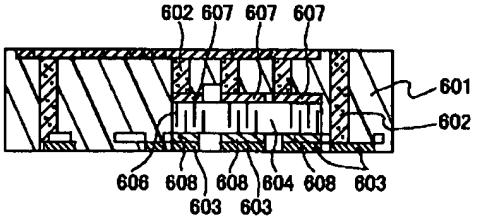
[Drawing 4]



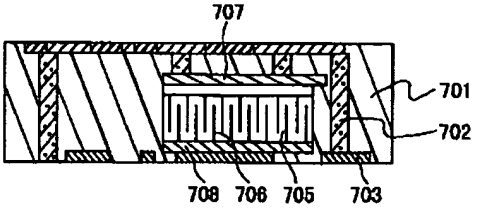
[Drawing 5]



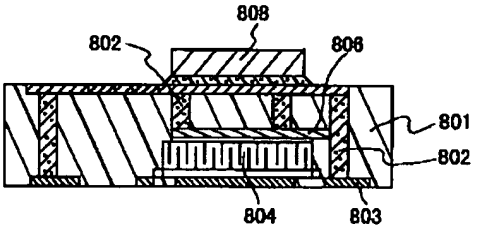
[Drawing 6]



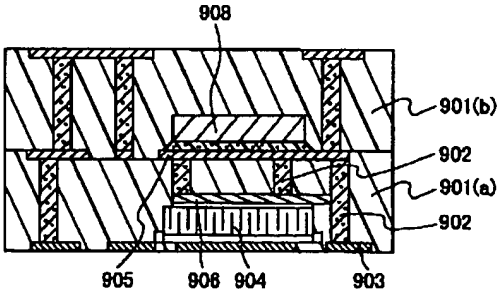
[Drawing 7]



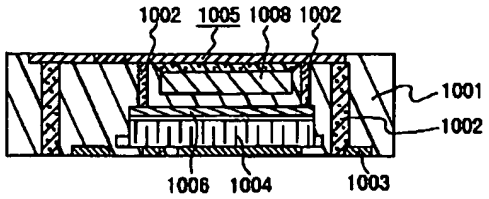
[Drawing 8]



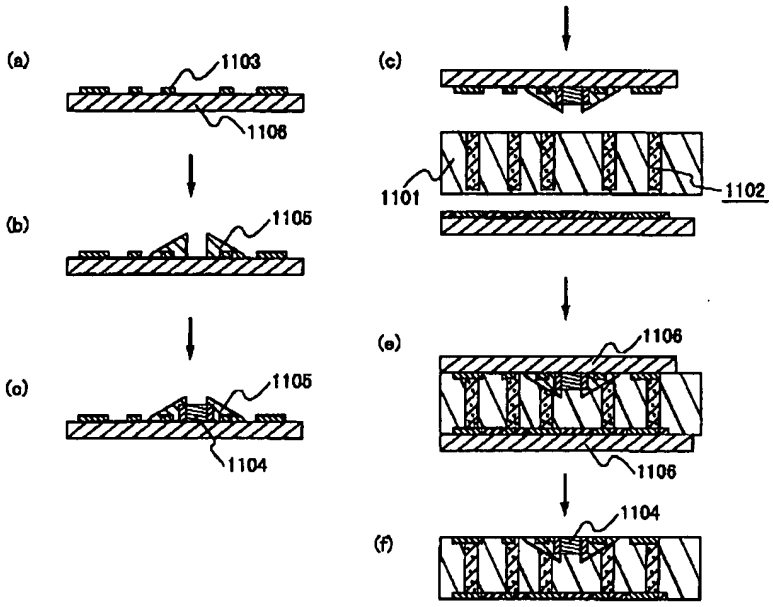
[Drawing 9]



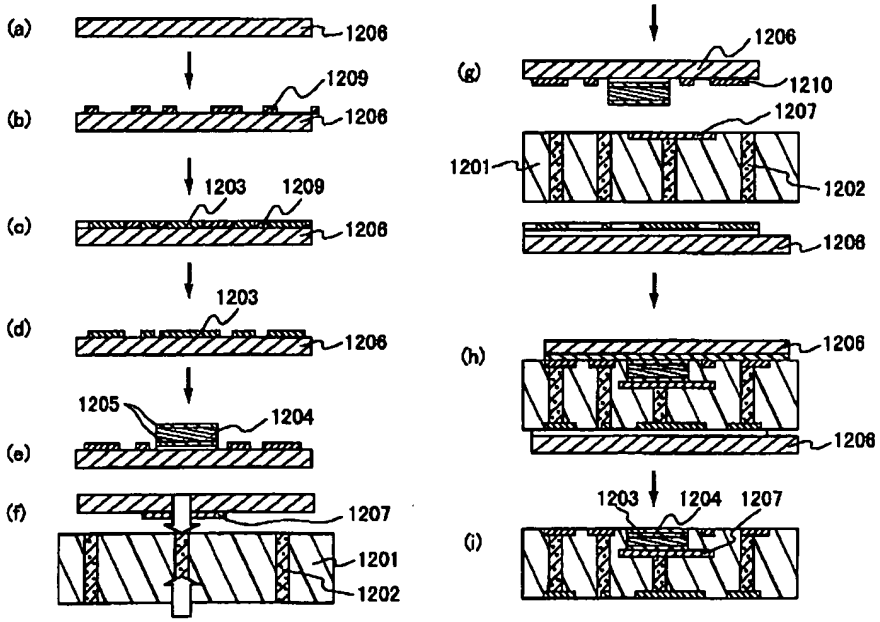
[Drawing 10]



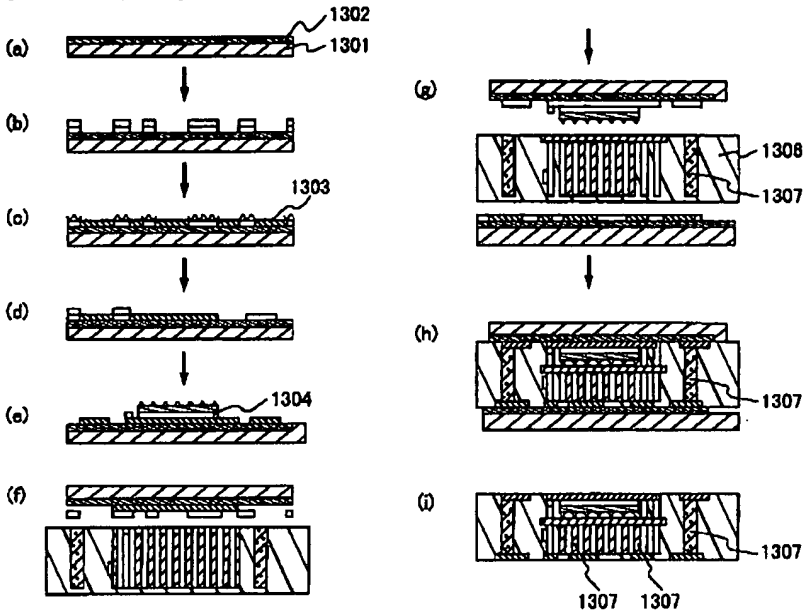
[Drawing 11]



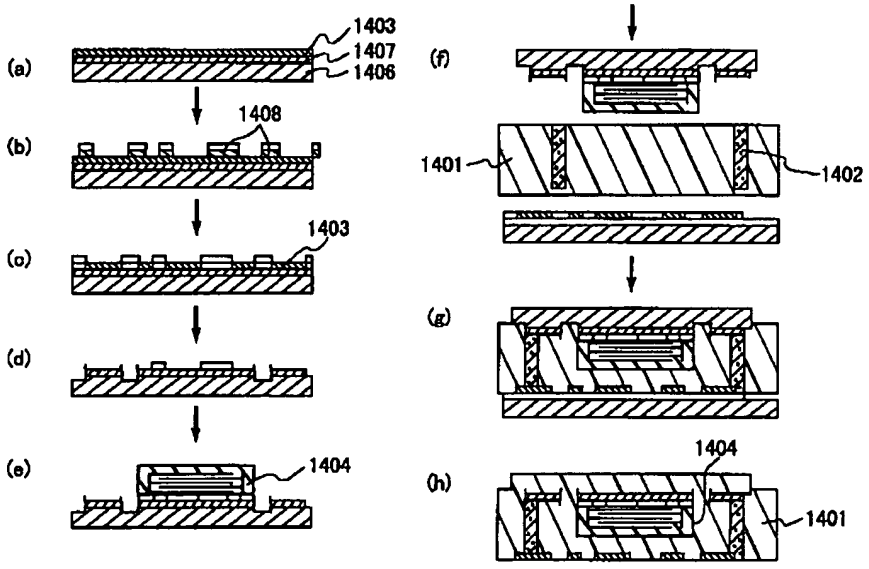
[Drawing 12]



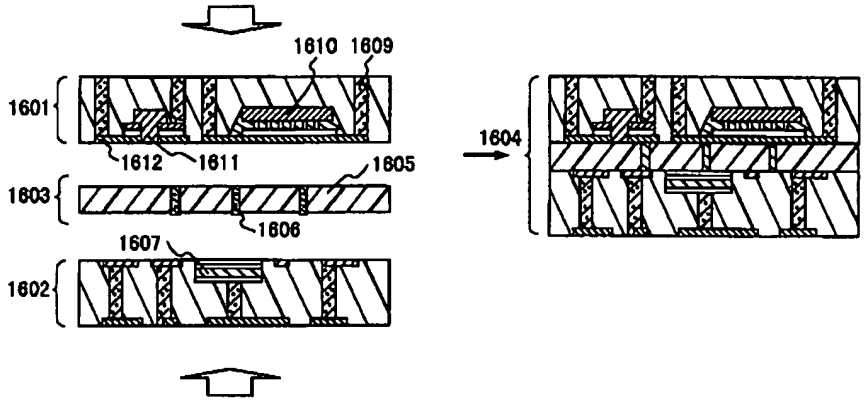
[Drawing 13]



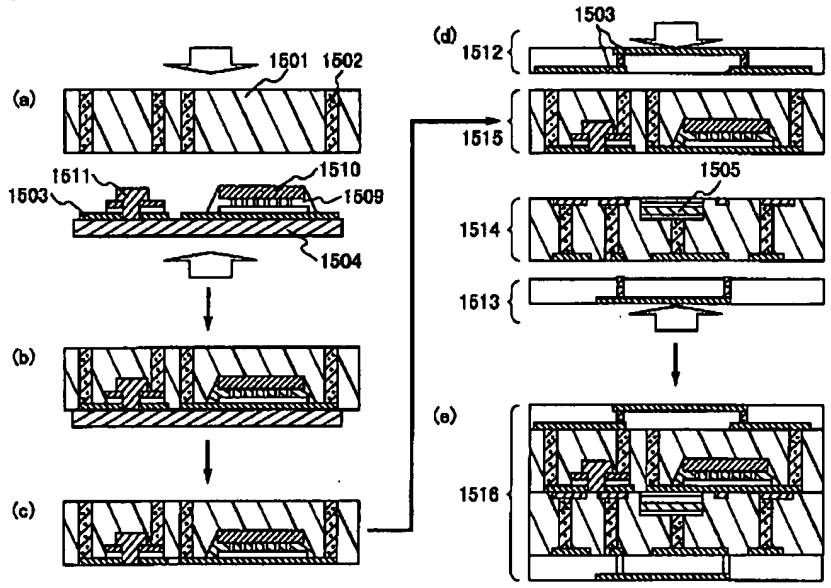
[Drawing 14]



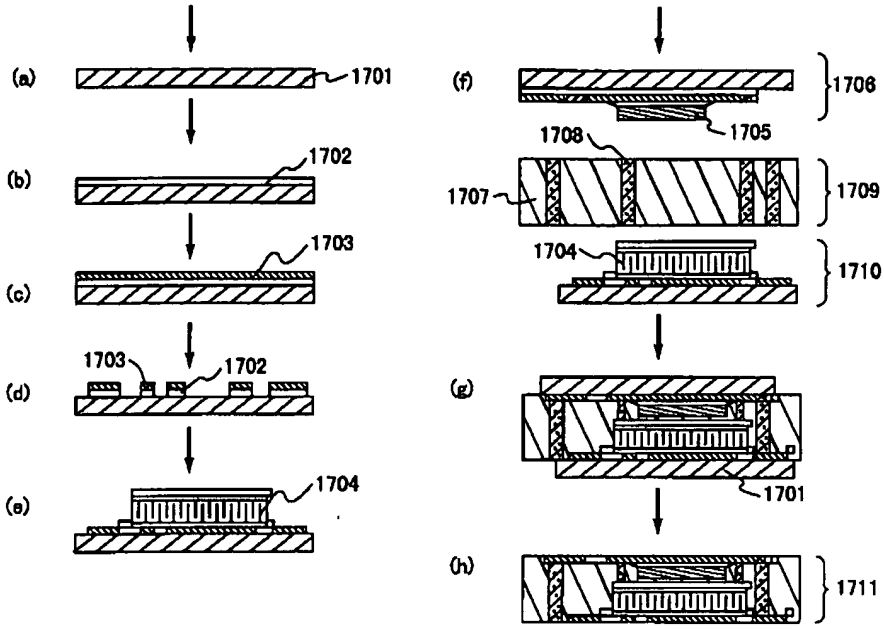
[Drawing 16]



[Drawing 15]



[Drawing 17]



[Translation done.]

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					Ｂ　５Ｅ３４３
	1/03	６１０		1/03	６１０Ｒ　５Ｅ３４６
	1/18			1/18	Ｒ
	3/20			3/20	Ｂ

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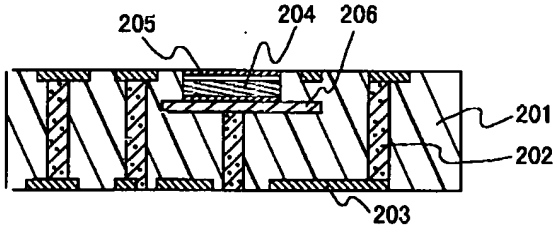
最終頁に続く

(54)【発明の名称】　チップ部品内蔵基板及びその製造方法

(57)【要約】
【課題】チップ部品を基板に内蔵するにあたって実装面積が小さく、部品内蔵層厚が薄くできる部品構成、及び回路基板に微細な配線パターンを形成しつつ、配線パターンとの接続を形成しながらＬＣＲ等のチップ受動部品を正確に実装、内蔵する製造方法を提供する。
【解決手段】上下面の少なくとも一方に電極が形成され、かつ１つ以上のチップ部品を内蔵し、チップ受動素子204の厚みｔが長さＬ及び幅Ｗより小さく、かつ前記チップ部品が、その厚み方向に対し上下面に対応する面内の少なくとも一方に、外部接続電極205を有し、外部接続電極205と電気絶縁性多層配線基板201に形成された配線パターン203が電気的に接続されている。



【特許請求の範囲】

【請求項１】上下面の少なくとも一方に電極が形成され、かつ１つ以上のチップ部品を内蔵した電気絶縁性配線基板であって、

前記チップ受動素子の厚みｔが長さＬ及び幅W以下であり、かつ前記チップ部品が、その厚み方向に対し上下面に対応する面内の少なくとも一方に、外部接続電極を有し、

前記外部接続電極と前記電気絶縁性多層配線基板に形成された配線パターンが電気的に接続されていることを特徴とするチップ部品内蔵配線基板。

【請求項２】前記電気絶縁性基板に半導体素子を含む能動素子がさらに内蔵されている請求項１に記載のチップ部品内蔵配線基板。

【請求項３】前記チップ部品が上下両面に電極が形成された単層チップコンデンサである請求項１に記載のチップ部品内蔵配線基板。

【請求項４】前記単層コンデンサの上下両面に形成された電極が、複数で構成されおり、かつ複数の静電容量を取り出すことができる請求項３に記載のチップ部品内蔵配線基板。

【請求項５】前記チップ部品が、内部に導体パターンで形成された受動素子を有する多層構造で構成されたチップ受動素子である請求項１に記載のチップ部品内蔵多層配線基板。

【請求項６】前記チップ部品が積層チップコンデンサである請求項１，２または５に記載のチップ部品内蔵配線基板。

【請求項７】前記積層チップコンデンサが、セラミックスからなる複数の誘電体層と前記誘電体層の内部に形成される内部電極及び内部電極と上面または下面に形成された外部端子電極が電気的に接続するように前記誘電体層を貫通するビアホール接続部を備えた請求項６に記載のチップ部品内蔵配線基板。

【請求項８】前記積層チップコンデンサにおいて、セラミック焼結体の下面と垂直な方向に沿ってセラミック層を介して重なり合うように配置された複数の内部電極とを備え、複数の内部電極は、静電容量を取り出すために、その端円の一部がセラミック焼結体の上面及び下面に露出されており、前記セラミック焼結体の上面に形成された第一の外部電極と、セラミック焼結体の下面に形成された少なくとも１つの第２の外部電極とをさらに備えて静電容量を取り出すことができる請求項５に記載のチップ部品内蔵配線基板。

【請求項９】前記積層チップコンデンサの第１の外部電極及び第２の外部電極がそれぞれ複数で構成されており、かつ複数の静電容量を取り出すことができる請求項８に記載のチップ部品内蔵配線基板。

【請求項１０】前記チップ受動素子の厚みが０．１ｍｍ以上０．５ｍｍ以下の範囲である請求項１に記載のチップ部品内蔵多層配線基板。

【請求項１１】前記電気絶縁性基板が、無機フィラーと熱硬化性樹脂組成物とを含み、少なくとも一つの貫通孔を有し、前記貫通孔に導電性ペーストが充填されている請求項１に記載のチップ部品内蔵配線基板。

【請求項１２】前記無機フィラーが、Al_2O_3、ＭｇＯ、ＢＮ、ＡＩＮおよびSiO_2から選択された少なくとも一つのフィラーであり、その無機フィラーの割合が７０～９５重量％であり、かつ熱硬化性樹脂組成物の割合が５～３０重量％である請求項１１に記載のチップ部品内蔵多層配線基板。

【請求項１３】前記電気絶縁性基板が、ガラス繊維の織布、ガラス繊維の不織布、耐熱有機繊維の織布および耐熱有機繊維の不織布からなる群から選択された少なくとも一つの補強材とその補強材に熱硬化性樹脂組成物を含浸したものからなり、少なくとも一つの貫通孔を有し、前記貫通孔に導電性ペーストが充填されている請求項１に記載のチップ部品内蔵配線基板。

【請求項１４】前記チップ受動素子が導電性接着剤で実装された請求項１に記載のチップ部品内蔵配線基板。

【請求項１５】前記半導体素子を含むチップ部品内蔵多層配線基板において、前記チップコンデンサ内蔵配線層と前記半導体素子とがデカップリングを行い、ビアまたはバンプを介して接続された請求項２，３または６に記載のチップ部品内蔵配線基板。

【請求項１６】半導体素子を含むチップ部品内蔵多層配線基板において、前記チップコンデンサ内蔵配線層と前記半導体素子が内蔵された配線層とがデカップリングを行い、ビアまたはバンプを介して接続された多層構造を有する請求項１５に記載のチップ部品内蔵配線基板。

【請求項１７】半導体素子及びチップ部品を内蔵した配線基板において、前記チップコンデンサ及び前記半導体素子が同一層内に内蔵されかつそれぞれの素子が、ビアまたはバンプを介してデカップリングを行い、接続された請求項１５に記載のチップ部品内蔵配線基板。

【請求項１８】前記チップ受動素子の厚みｔが、長さＬの５～９０％であり、かつ前記チップ受動素子の厚みｔが、幅Wの５～９０％である請求項１に記載のチップ部品内蔵配線基板。

【請求項１９】キャリア層に剥離層を介して金属層を直接付着させて配線パターン形状に加工し、転写用配線パターンを形成し、前記転写用配線パターン形状と位置合わせしながらチップ受動素子を実装した転写用部品配線パターン形成材を用いて、

前記部品配線パターンが形成された側が電気絶縁性基板を構成するシート状基材の少なくとも一方の表面と接触するように配置して、これらを接着して埋め込み、

前記転写用配線パターン金属層をキャリア層から剥離し、前記シート状基材に少なくとも金属層及びチップ部品を含む前記部品配線パターンを転写することを含むチ

ップ部品内蔵配線基板の製造方法。
【請求項２０】前記転写用配線パターンが、（ａ）キャリア層が、第１の金属層で構成され、前記第１の金属層上に剥離層を介して、第１の金属層と同一成分の金属を含む第２の金属層を形成して、３層構造を形成し、
（ｂ）第２の金属層のみを配線パターン形状に加工することを含む請求項１９に記載のチップ部品内蔵配線基板の製造方法。
【請求項２１】前記転写用配線パターンが、（ａ）キャリア層が、第１の金属層で構成され、前記第１の金属層上に剥離層を介して、第１の金属層と同一成分の金属を含む第２の金属層を形成して、３層構造を形成し、
（ｂ）第２の金属層と剥離層および前記第１の金属層の表層部の任意の深さまでを配線パターン形状に加工して、前記第１の金属層の表層部に凹凸部を形成することを含む請求項１９に記載のチップ部品内蔵配線基板の製造方法。
【請求項２２】（ａ）キャリア層が第１の金属層で構成され、前記第１の金属層上に第２の金属層を直接付着させて配線パターン形状に加工し、転写用配線パターンを形成し、（ｂ）前記配線パターン形状と位置合わせしながらチップ部品パターンを実装、形成する工程とを含んで形成される転写用部品配線パターン形成材を用いて、これの部品配線パターンが形成された側が電気絶縁性基板を構成するシート状基材の少なくとも一方の表面と接触するように配置して、これらを接着して埋め込み、
（ｃ）第２の金属層を含む前記転写用配線パターン金属層を第１の金属層から剥離し、前記シート状基材に少なくとも第２の金属層及び部品パターンを含む前記部品配線パターンを転写することをも含むチップ部品内蔵配線基板の製造方法。
【請求項２３】前記第２の金属層を直接付着させて配線パターン形状に加工する方法がメッキ法である請求項２２に記載のチップ部品内蔵配線基板の製造方法。
【請求項２４】前記チップ部品が前記転写用配線パターンに導電性接着剤を用いて実装されている請求項１９～２３のいずれかに記載のチップ部品内蔵配線基板の製造方法。
【請求項２５】請求項１９～２４のいずれかに記載の製造方法によって形成されたチップ部品内蔵配線基板を、一括積層によりさらに二層以上に積層したチップ部品内蔵配線基板の製造方法。
【請求項２６】キャリア層に剥離層を介して金属層を直接付着させて配線パターン形状に加工し、転写用配線パターンを形成し、
前記転写用配線パターン形状と位置合わせしながら半導体素子を実装した転写用部品配線パターン形成材を用いて、
前記素子配線パターンが形成された金属層側が電気絶縁性基板を構成するシート状基材の少なくとも一方の表面と接触するように配置して、これらを接着し、
前記転写用配線パターン金属層をキャリア層から剥離し、前記シート状基材に少なくとも金属層及び半導体素子を含む前記部品配線パターンを転写することを含む半導体内蔵配線基板と、前記チップ部品内蔵配線基板とを、ビアまたはバンプを介して接続してそれぞれがデカップリングされたチップ部品を得ることを特徴とするチップ部品内蔵配線基板の製造方法。
【請求項２７】前記半導体内蔵配線基板と前記チップ部品内蔵基板を、あらかじめＣステージ（完全硬化）に硬化した状態で用意し、各基板層をビアを介したＢステージ（半硬化）の配線層を介在させて積層し、半導体素子とチップ部品とを接続する請求項２６に記載のチップ部品内蔵配線基板の製造方法。
【請求項２８】キャリア層に剥離層を介して金属層を直接付着させて配線パターン形状に加工し、転写用配線パターンを形成し、前記転写用配線パターン形状と位置合わせしながら半導体素子を実装した転写用部品配線パターン形成材と、
キャリア層に剥離層を介して金属層を直接付着させて配線パターン形状に加工し、転写用配線パターンを形成し、前記転写用配線パターン形状と位置合わせしながらチップ部品を実装した転写用部品配線パターン形成材とを用いて、
これらの素子配線パターンが形成された側が電気絶縁性基板を構成するシート状基材のそれぞれ表裏両面の表面と接触するように配置して、これらを接着して埋め込み、
前記転写用配線パターン金属層をキャリア層から剥離し、前記シート状基材に少なくとも金属層及び半導体素子を含む前記部品配線パターンを転写した半導体内蔵配線基板と、前記チップ部品内蔵配線基板とを、ビアまたはバンプを介して接続し、それぞれがデカップリングされたチップ部品を得ることを特徴とするチップ部品内蔵配線基板の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、転写用部品配線パターン形成材を用いて、部品配線パターンが形成されたチップ部品からなる受動部品が内蔵された配線基板とその製造方法に関するものである。
【０００２】
【従来の技術】近年、電子機器の高性能化、小型化、高周波化の要求に伴い、半導体のさらなる高密度、高機能化が要請されている。このため、前記半導体の他にコンデンサ（Ｃ）、インダクタ（Ｌ）、抵抗（Ｒ）等の受動部品自体も小型化しており、さらにこれら特性が保証されたチップ受動部品を実装するための回路基板も、さらに小型高密度なものが必要とされている。
【０００３】これらの要求に対し、例えば、ＬＳＩ間や

実装部品間の電気配線を、最短距離で接続できる基板層間の電気接続方式であるインナービアホール（ＩＶＨ）接続法が、最も回路の高密度配線化が可能であることから、各方面で開発が進められている。一般に、このようなＩＶＨ構成の配線基板としては、例えば、多層セラミック配線基板、ビルドアップ法による多層プリント配線基板、樹脂と無機フィラーとの混合物からなる多層コンポジット配線基板等があげられる。

【０００４】前記多層セラミック配線基板は、例えば、以下に示すようにして作製できる。まず、アルミナ等のセラミック粉末、有機バインダおよび可塑剤からなるグリーンシートを複数枚準備し、前記各グリーンシートにビアホールを設け、前記ビアホールに導電性ペーストを充填した後、このグリーンシートに配線パターン印刷を行い、前記各グリーンシートを積層する。そして、この積層体を、脱バインダおよび焼成することにより、前記多層セラミック配線基板を作製できる。このような多層セラミック配線基板は、ＩＶＨ構造を有するため、極めて高密度な配線パターンを形成でき、電子機器の小型化等に最適である。

【０００５】また、この多層セラミック配線基板の構造を模した、前記ビルドアップ法によるプリント配線基板も各方面で開発されている。例えば、特開平９－１１６２６７号公報、特開平９－５１１６８号公報等には、一般的なビルドアップ法として、従来から使用されているガラス－エポキシ基板をコアとし、この基板表面に感光性絶縁層を形成した後、フォトリソグラフィー法でビアホールを設け、さらにこの全面に銅メッキを施し、前記銅メッキを化学エッチングして配線パターンを形成する方法が開示されている。

【０００６】また、特開平９－３２６５６２号公報には、前記ビルドアップ法と同様に、前記フォトリソグラフィー法により加工したビアホールに、導電性ペーストを充填する方法が開示され、特開平９－３６５５１号公報、特開平１０－５１１３９号公報等には、絶縁性硬質基材の一表面に導体回路を、他方表面に接着剤層をそれぞれ形成し、これに貫通孔を設けて、導電性ペーストを充填した後、複数の基材を重ねて積層する多層化方法が開示されている。

【０００７】また、特許第２６０１１２８号、特許第２６０３０５３号、特許第２５８７５９６号は、アラミド－エポキシプリプレグにレーザ加工により貫通孔を設け、ここに導電性ペーストを充填した後、銅箔を積層してパターニングを行い、この基板をコアとして、導電性ペーストを充填したプリプレグでさらに挟み多層化する方法である。

【０００８】以上のように、例えば、樹脂系プリント配線基板をＩＶＨ接続させれば、前記多層セラミック配線基板と同様に、必要な各層間のみの電気的接続が可能であり、さらに、配線基板の最上層に貫通孔がないため、より実装性にも優れる。

【０００９】しかしながら上記のように、高密度配線化された多層配線基板においても、コンデンサ、抵抗器など配線基板の表面に実装される電子部品の占める割合は依然として高く、電子機器の小型化に対して、大きな課題となっている。このような課題の解決策として配線基板内に電子部品を埋設して高密度実装化を図ろうとする提案が開示されている。

【００１０】例えば、プリント基板に設けた透孔内にリードレス部品を埋設した特開昭５４－３８５６１号公報、絶縁基板に設けた貫通孔内にセラミックコンデンサ等の受動素子を埋設した特公昭６０－４１４８０号公報、半導体素子のバイパスコンデンサをプリント配線基板の孔に埋設した特開平４－７３９９２号公報および特開平５－２１８６１５号公報等が開示されている。

【００１１】また、セラミック配線基板に設けたビアホール内に導電性物質と誘電性物質を充填して同時焼成した特開平８－２２２６５６号公報、有機系絶縁基板に設けた貫通孔に電子部品形成材料を埋め込んだ後、固化させてコンデンサや抵抗器を形成した特開平１０－５６２５１号公報等が開示されている。

【００１２】上記従来の開示技術はいずれも二つの方式に大別できる。すなわちその一つは配線基板に設けられた貫通孔にチップ抵抗器またはチップコンデンサ等の既に完成されたリードレス部品を埋設した後、このリードレス部品の電極と配線基板上の配線パターンとを導電性ペイントまたは半田付けによって接続するものである。また、他の一つは有機系配線基板の場合、配線基板に設けた貫通孔にコンデンサ等の電子部品形成材料を埋め込み、固化させることによって所望のコンデンサとした後、その上下の端面にメッキを施して電極を形成して電子部品内蔵配線基板を形成させ、また無機系配線基板の場合は、セラミックグリーン　に設けられたビアホール内に誘電体ペーストや導電性ペーストを充填した後、高温で焼成することにより、所望のコンデンサを内蔵した配線基板を形成したものである。

【００１３】しかしながら、これらの貫通孔を利用して焼成あるいは固化したコンデンサで大容量を得ることは困難である。一方、あらかじめ、大容量が確保されているチップコンデンサ等を貫通孔を利用して埋設、実装する場合は、現行、最小サイズの０６０３チップを用いた場合でも０．６ｍｍの層厚みが必ず伴い、薄い多層基板を実現することが困難となる。

【００１４】また、チップ部品単体でみた場合、市場には、１００５，０６０３に代表される側面に電極が構成されたチップ部品が代表的であり、それらを基板に内蔵した例は、特開平11-220262号公報（米国特許第6,038,133号明細書）などに既に提案されているが、内蔵用に特性、形状を考慮して構造を対応させたもの、またそれを基板に内蔵させた形態は、まだ提案されていない。さら

に、チップ部品単体でみた場合、上下面に電極を有する素子としては、単層チップコンデンサや薄膜積層コンデンサがあるが、これらはいずれも表面実装する事しか想定されておらず、電極間をワイヤーボンドで接続したり、リボンリードで接続したりすることが一般的に用いられている。従って、これらチップ部品を基板に内蔵することや、及び内蔵させたときに配線パターンと精度良く接続させる有効な製造方法は未だ提案されていなかった。

【００１５】一方、ＩＶＨ構造を有する高密度実装の樹脂系プリント配線基板は、一般に熱伝導度が低く、部品の実装が高密度になるに従って、前記部品から発生する熱を放熱させることは、特に半導体素子等の能動部品を実装、あるいは内蔵した場合は困難となる。

【００１６】西暦２０００年には、ＣＰＵのクロック周波数が、１ＧＨｚ程度になり、その機能の高度化に伴い、ＣＰＵの消費電力も、１チップ当たり１００～１５０Ｗに達すると推測される。そのため、部品を内蔵させる基板には高熱伝導性が要求されつつある。

【００１７】この観点で基板をみた場合、セラミック配線基板が比較的高価であることや、樹脂系プリント配線基板が熱伝導性に課題を有すること等を補完する目的で、多層コンポジット配線基板が、特開平９－２７０５８４号公報、特開平８－１２５２９１号公報、特開平８－２８８５９６号公報、特開平１０－１７３０９７号公報等に提案されている。この多層コンポジット配線基板は、エポキシ樹脂等の熱硬化性樹脂と、熱伝導性に優れる無機フィラー（例えば、セラミック粉末等）とを混合し、複合化させた基板であり、前記無機フィラーを高濃度に含有することが可能なため、前記基板の熱伝導性を向上できる。また、前記無機フィラーの種類を選択することにより、例えば、誘電率、熱膨張係数等を任意に制御することが可能である。

【００１８】一方、基板の高密度実装を進める上で、重要なのが微細な配線パターンの形成及び、その配線パターンと接続されたＬＣＲの形成、実装である。前記多層セラミック配線基板において、配線パターンの形成は、例えば、セラミック基板に厚膜導電性ペーストをスクリーン印刷し、焼成により焼き固める方法が一般的に利用されている。しかし、このスクリーン印刷法では、１００μｍ以下の線幅である配線パターンを量産することは困難であると言われている。また、ＬＣＲ等の受動部品は、表面実装する方法に限定されており、基板内に内蔵させることは困難であった。また、セラミック基板では焼成工程が伴うため、特性の保証されている安価に入手できるチップ部品を内蔵させること不可能であった。この意味でも、高密度実装に限界が生じていた。

【００１９】また、通常のプリント配線基板においては、例えば、サブトラクティブ法により配線パターンを形成する方法が一般的である。このサブトラクティブ法では、厚み１８～３５μｍ程度の銅箔を、化学エッチングすることにより、基板に配線パターンを形成するが、この方法でも７５μｍ以下の線幅である配線パターンを量産することは困難であると言われており、前記配線パターンをさらに微細化するためには、前記銅箔を薄くする必要がある。

【００２０】また、前記サブトラクティブ法によれば、基板表面に配線パターンが突出した構造となるため、半導体に形成したバンプ上に、電気接続のための半田や導電性接着剤等を乗せ難く、また、前記バンプが配線パターン間に移動して、ショートするおそれもある。また、前記突出した配線パターンのため、例えば、後の工程で、封止樹脂で封止する際の障害となるおそれもある。

【００２１】また、前記ビルドアップ法によるプリント配線基板においては、前記サブトラクティブ法以外に、例えば、アディティブ法が採用される傾向にある。このアディティブ法は、例えば、レジストを形成した基板表面に、配線パターンを選択的にメッキする方法であり、３０μｍ程度の線幅である配線パターンを形成することができる。しかし、この方法は、前記サブトラクティブ法に比べ、基板に対する配線パターンの密着強度が弱い等の問題がある。

【００２２】そこで、予め微細な配線パターンを形成し、パターン検査を行った後、良品の配線パターンだけを、所望の基板に転写する方法が考案されている。例えば、米国特許５，４０７，５１１号は、予めカーボン板の表面に、微細パターンを印刷および焼成によって形成し、これをセラミック基板に転写する方法である。

【００２３】また、特開平１０－８４１８６号公報、特開平１０－４１６１１号公報には、離型性支持板上に形成した銅箔からなる配線パターンを、プリプレグに転写する方法が開示され、同様に特開平１１－２６１２１９には、銅箔で構成された離型性支持板上にニッケルリン合金剥離層を介して銅箔からなる配線パターンを転写する方法が、また特開平８－３３０７０９号公報には、配線パターンである銅箔の粗化面および光沢面における接着度合いが、それぞれ異なることを利用して基板に転写する方法が、開示されている。

【００２４】このような転写法により転写される配線パターンは、基板表面に埋め込まれ、得られる配線基板の表面が平坦な構造となるため、前述のように配線パターンの突出による問題は回避される。さらに、特開平１０－１９０１９１公報では、配線パターンを基板表面に埋め込む際に、貫通孔に充填させた導電性ビアペーストを前記配線パターンの厚み分だけ圧縮する効果も開示されている。

【００２５】

【発明が解決しようとする課題】しかし、これらの方法では、転写形成材の上に形成されたパターンは、いずれも銅箔等の配線部分だけである。さらに高密度に実装す

るため、ＬＣＲ等をチップの形態で転写形成材の上に実装させる提案もできるが、現行のチップでは、側面に電極が形成されているため、ハンダーリフロー等で実装させると、部品面積と比較してかなり大きな実装接続面積が要求される。それを防ぐため、転写形成材上に電極が垂直になるようにチップを立てた状態で実装して基板に転写、内蔵させるためには、埋め込み時にチップの位置ずれ、チップ部品の長さ分以上の厚い層厚の確保等、様々な問題が生じ、多層基板の設計上、限定が多くなる。また、転写形成材上にワイヤーボンドで実装して、転写内蔵させる場合は、あらかじめその領域を樹脂封止して保護した後埋め込むことになる。但しワイヤーボンドで接続した場合、部品間の配線が長くなるため、高周波用途では特性が劣化してしまうことが報告されている。

【００２６】そこで、本発明は、チップ部品を基板に内蔵するにあたって実装面積が小さく、部品内蔵層厚が薄くできる部品構成、及び回路基板に微細な配線パターンを形成しつつ、配線パターンとの接続を形成しながらＬＣＲ等のチップ受動部品を正確に実装、内蔵する製造方法を提供することを目的とする。

【００２７】

【課題を解決するための手段】前記目的を達成するために、本発明者らは、厚みの薄い上下面いずれかに電極が形成されたチップ受動素子を提案し、それらを転写形成材を用いることによって正確に実装、埋め込むことができるため、高周波用途に適合した最短配線で薄いチップ部品内蔵配線基板を提供する。

【００２８】すなわち本発明のチップ部品内蔵配線基板は、上下面の少なくとも一方に電極が形成され、かつ１つ以上のチップ部品を内蔵した電気絶縁性配線基板であって、前記チップ受動素子の厚みｔが長さL及び幅W以下であり、かつ前記チップ部品が、その厚み方向に対し上下面に対応する面内の少なくとも一方に、外部接続電極を有し、前記外部接続電極と前記電気絶縁性多層配線基板に形成された配線パターンが電気的に接続されていることを特徴とする。

【００２９】次に本発明の第１番目の方法は、キャリア層に剥離層を介して金属層を直接付着させて配線パターン形状に加工し、転写用配線パターンを形成し、前記転写用配線パターン形状と位置合わせしながらチップ受動素子を実装した転写用部品配線パターン形成材を用いて、前記部品配線パターンが形成された側が電気絶縁性基板を構成するシート状基材の少なくとも一方の表面と接触するように配置して、これらを接着して埋め込み、前記転写用配線パターン金属層をキャリア層から剥離し、前記シート状基材に少なくとも金属層及びチップ部品を含む前記部品配線パターンを転写することを含むチップ部品内蔵配線基板の製造方法である。

【００３０】次に本発明の第２番目の方法は、（ａ）キャリア層が第１の金属層で構成され、前記第１の金属層上に第２の金属層を直接付着させて配線パターン形状に加工し、転写用配線パターンを形成し、（ｂ）前記配線パターン形状と位置合わせしながらチップ部品パターンを実装、形成する工程とを含んで形成される転写用部品配線パターン形成材を用いて、これの部品配線パターンが形成された側が電気絶縁性基板を構成するシート状基材の少なくとも一方の表面と接触するように配置して、これらを接着して埋め込み、（ｃ）第２の金属層を含む前記転写用配線パターン金属層を第１の金属層から剥離し、前記シート状基材に少なくとも第２の金属層及び部品パターンを含む前記部品配線パターンを転写することをも含むチップ部品内蔵配線基板の製造方法である。

【００３１】次に本発明の第３番目の方法は、キャリア層に剥離層を介して金属層を直接付着させて配線パターン形状に加工し、転写用配線パターンを形成し、前記転写用配線パターン形状と位置合わせしながら半導体素子を実装した転写用部品配線パターン形成材を用いて、前記素子配線パターンが形成された金属層側が電気絶縁性基板を構成するシート状基材の少なくとも一方の表面と接触するように配置して、これらを接着し、前記転写用配線パターン金属層をキャリア層から剥離し、前記シート状基材に少なくとも金属層及び半導体素子を含む前記部品配線パターンを転写することを含む半導体内蔵配線基板と、前記チップ部品内蔵配線基板とを、ビアまたはバンプを介して接続してそれぞれがデカップリングされたチップ部品を得ることを特徴とするチップ部品内蔵配線基板の製造方法である。

【００３２】次に本発明の第４番目の方法は、キャリア層に剥離層を介して金属層を直接付着させて配線パターン形状に加工し、転写用配線パターンを形成し、前記転写用配線パターン形状と位置合わせしながら半導体素子を実装した転写用部品配線パターン形成材と、キャリア層に剥離層を介して金属層を直接付着させて配線パターン形状に加工し、転写用配線パターンを形成し、前記転写用配線パターン形状と位置合わせしながらチップ部品を実装した転写用部品配線パターン形成材とを用いて、これらの素子配線パターンが形成された側が電気絶縁性基板を構成するシート状基材のそれぞれ表裏両面の表面と接触するように配置して、これらを接着して埋め込み、前記転写用配線パターン金属層をキャリア層から剥離し、前記シート状基材に少なくとも金属層及び半導体素子を含む前記部品配線パターンを転写した半導体内蔵配線基板と、前記チップ部品内蔵配線基板とを、ビアまたはバンプを介して接続し、それぞれがデカップリングされたチップ部品を得ることを特徴とするチップ部品内蔵配線基板の製造方法である。

【００３３】

【発明の実施の形態】本発明は、上下面少なくともいずれか一方に電極が形成されたチップ受動素子を内蔵した電気絶縁性多層配線基板であって、前記チップ受動素子

の厚みｔが長さL及び幅Wより小さく設定され、その厚み方向に対し上下面に対応する面内の少なくともいずれか一方に、面内に収まる外部接続電極を有し、前記外部接続電極と前記電気絶縁性多層配線基板に形成された配線パターンが接続されたチップ部品内蔵多層配線基板である。

【００３４】これは、通常のチップ部品を内蔵した基板と異なり、上下面に電極が構成されているために、実装に伴う新たな面積が発生せず、且つ厚みの薄いチップ部品を採用しているため、体積効率の極めて高い小型、薄型化されたチップ部品内蔵基板を形成することができる。

【００３５】前記においては、前記電気絶縁性基板に半導体素子を含む能動素子がさらに内蔵されていることが好ましい。

【００３６】また、前記チップ受動素子が上下両面に電極が形成された単層チップコンデンサであると、きわめて薄く、かつ小面積化が可能となる。さらに、単層チップコンデンサの容量スペックは、通常の積層チップコンデンサより１０倍以上正確な値を実現でき、設計の厳しい高周波での用途で効果を発揮できる。

【００３７】また、前記単層コンデンサの上下両面に形成された電極構成が、二つ以上の複数で構成されおり、その結果として複数の静電容量を取り出すことができる。

【００３８】また、前記チップ受動素子が、内部に導体パターンで形成された受動素子を有する多層基板で構成されたチップ部品であり、例えば、積層チップインダクター、積層チップコンデンサ等に対応し、品質が保証された大インダクタンス、大容量を有するチップ部品内蔵基板を実現することができる。

【００３９】また、積層チップコンデンサが、セラミックスからなる複数の誘電体層と該誘電体層の内部に形成される内部電極及び内部電極と上面あるいは下面に形成された外部端子電極が電気的に接続するように前記誘電体層を貫通するビアホール接続部を備えたことが好ましい。従って、下面電極のみで接続端子を取り出すことができる点、及び従来の側面電極の場合と比較して端子電極と内部積層電極との距離が短い構造となるため、浮遊容量を小さくすることができ、正確な容量を導出しやすい点が利点として挙げられる。

【００４０】また、積層チップコンデンサにおいて、セラミック焼結体の下面と垂直な方向に沿ってセラミック層を介して重なり合うように配置された複数の内部電極とを備え、複数の内部電極は、静電容量を取り出すために、その端円の一部がセラミック焼結体の上面及び下面に露出されており、前記セラミック焼結体の上面に形成された第一の外部電極と、セラミック焼結体の下面に形成された少なくとも１つの第２の外部電極とをさらに備えて静電容量を取り出すことができる。従って、ビアホール接続部を用いずに上下面に端子電極を構成することができるため、容易にチップコンデンサを作製することができる。また、積層構造を採用しているため、大容量のコンデンサを得ることができ且つ、厚みの伴わないチップコンデンサ内蔵基板を得ることができる。

【００４１】また、前記積層コンデンサの上下両面に形成された電極構成が、二つ以上の複数で構成されおり、その結果として複数の静電容量を取り出すことができる。

【００４２】また、チップ受動素子の厚みが０．１ｍｍ以上であれば、割れ等を生じさせないように取り扱うことでき、一方０．５ｍｍ以下の範囲であると、チップ部品を内蔵した層厚を抑えることができる。

【００４３】また、電気絶縁性基板が、無機フィラーと熱硬化性樹脂組成物とを含み、少なくとも一つの貫通孔を有し、前記貫通孔に導電性ペーストが充填されていると、かとう性に優れ、チップ部品を容易に埋め込むことができる。

【００４４】また、無機フィラーが、Al_2O_3、ＭｇＯ、ＢＮ、ＡｌＮおよびSiO_2からなる群から選択された少なくとも一つの無機フィラーであり、その無機フィラーの割合が７０～９５重量％であり、熱硬化性樹脂組成物の割合が５～３０重量％であるのが好ましい。この例によれば、無機フィラーが極めて高密度に充填されているので、例えば無機フィラーにAl_2O_3を選べば一般有機系樹脂基板と比較して高熱伝導な基板が得られ、無機フィラーの特性を生かすことができる。

【００４５】また、絶縁性基板が、ガラス繊維の織布、ガラス繊維の不織布、耐熱有機繊維の織布および耐熱有機繊維の不織布からなる群から選択された少なくとも一つの補強材とその補強材に熱硬化性樹脂組成物を含浸したものからなり、少なくとも一つの貫通孔を有し、前記貫通孔に導電性ペーストが充填されているものでもよい。

【００４６】また、チップ受動素子が導電性接着剤で実装されたものであり、非鉛系材料のチップ部品を採用すれば、完全に非鉛系のチップ部品内蔵基板を作製することができる。

【００４７】また、チップコンデンサ内蔵配線層と前記半導体素子とがデカップリングを行い、ビアまたはバンプを介して接続された構造であると、半導体素子とチップコンデンサとの最短距離実装が実現されており、低ノイズ化等の優れた特性を有するデバイスを実現できる。ここで、デカップリングとは、ＩＣの動作事に発生する高周波雑音を極力ＩＣ周辺の高速回路内に閉じ込めて外部のプリント基板やケーブルに流さないようにすることをいう。

【００４８】また、チップコンデンサ内蔵配線層と前記半導体素子が内蔵された配線層とがデカップリングを行い、ビアまたはバンプを介して接続された構造である

と、半導体素子とチップコンデンサとの最短距離実装の実現及び最大限の体積効率化が実現され、積層内蔵基板全体の薄型化を実現することができる。

【００４９】また、前記チップコンデンサ及び前記半導体素子が同一層内に内蔵され且つそれぞれの素子が、ビアまたはバンプを介してデカップリングを行い、接続された構造が好ましい。この例によれば、半導体素子とチップコンデンサとの最短距離実装の実現及び最大限の体積効率化が実現された、内蔵基板全体の薄型化、さらに前記チップコンデンサ及び前記半導体素子の内蔵プロセスを同時に行うことができ、工程を簡略化させることができる。

【００５０】本発明においては、前記チップ受動素子の厚みｔは、長さLの５～１００％が好ましく、さらに５～９０％が好ましく、とくに２０～７０％の範囲が好ましい。前記チップ受動素子の厚みｔは、幅Wの５～１００％が好ましく、さらに５～９０％が好ましく、とくに２０～７０％の範囲が好ましい。より具体的には、チップ受動素子の長さLは０．２ｍｍ～２．３ｍｍの範囲が好ましく、幅Wは０．２ｍｍ～２．５ｍｍの範囲が好ましい。

【００５１】次に本発明の第１番目の方法によれば、容易にチップ部品を基板内に実装することができる。

【００５２】また本発明の第２番目の方法によれば、たとえば、銀配線パターンと接続されたチップ部品を容易に基板内に実装することができる。

【００５３】前記方法において、第２の金属層を直接付着させて配線パターン形状に加工する方法がメッキ法である例によれば、ファインパターンを容易に実現することができる。

【００５４】また、チップ部品が前記転写用配線パターンに導電性接着剤を用いて実装する例によれば、非鉛系の部品内蔵配線基板の実現を可能にできる。

【００５５】また、一括積層によりさらに二層以上に積層すると、容易に部品内蔵基板を積層する事ができる。

【００５６】次に本発明の第３番目の方法によれば、半導体内蔵基板とチップ部品内蔵基板を容易に互いに電気的に接続させながら積層させることができる。

【００５７】次に本発明の第４番目の方法によれば、半導体素子とチップ部品を同時に内蔵させることができるので、製造工程を簡略化することができる。

【００５８】前記方法において、半導体内蔵配線基板と前記チップ部品内蔵基板を、あらかじめＣステージに硬化した状態で用意し、各基板層をビアを介したＢステージの配線層を介在させて積層することによって、次工程である積層工程で内蔵された部品をより強固に保護することができる。

【００５９】なお、本発明において基板とは、配線パターンを形成する前のシート状基材等をいい、配線基板とは、前記基板に配線パターンを形成したものをいい、回路基板とは、前記基板に配線パターンのみならず、半導体チップ等の能動部品またはＬＣＲ等受動部品を実装したものを示す。

【００６０】

【発明の実施の形態】（実施の形態１）本発明の第１の実施の形態であるチップ部品内蔵基板の一例の構成概略を、従来提案されている形態、図１と比較しながら図２に示す。

【００６１】図１(a)に示すように、従来のチップ部品内蔵基板の形態は、埋め込まれたチップ部品１０４と基板１０１に形成されたビア接続部１０２、配線部１０３とがワイヤーボンド１０５で接続された構造であったり、図１（ｂ）で示されるように、埋め込まれたチップ部品１０４と基板１０１に形成されたビア接続部１０２、配線部１０３とが半田１０６で接続された構造である。図１(a)のワイヤーボンド接続構造では、配線長が長くなるため、特に高周波域での特性に問題が生じる。一方、図１（ｂ）の半田接続構造では、配線長の問題はやや回避できるものの、半田リフローに要する実装面積がチップ部品に対し大きくなり高密度実装に弊害となっている。

【００６２】これに対し、図２のように、前記第１の実施形態であるチップ部品内蔵基板では、内蔵されたチップ部品２０４が上下面少なくともいずれか一方に電極が形成されていて、前記チップ受動素子２０４の厚みｔが長さL及び幅Wより小さく設定され、その厚み方向に対し上下面に対応する面内の少なくともいずれか一方に、面内に収まる外部接続電極２０５を有し、前記外部接続電極２０５と前記電気絶縁性多層配線基板２０１に形成された配線パターン２０３とが接続された構成となる。

【００６３】前記チップ受動素子２０４は例えば、単層チップコンデンサが考えられる。単層チップコンデンサの外形寸法は、０．２５ｍｍ角から２．５ｍｍ角オーダーまで、厚みは８０μｍから３００μｍまで容量に応じて網羅されており、通常の積層チップコンデンサと比較して極めて薄く、正確な容量値を導出することができる。従って、内蔵に伴い、基板の層厚を特に厚くする必要がなく高密度チップ部品内蔵多層基板に最適である。

【００６４】単層チップコンデンサを構成する誘電体材料は、チタン酸バリウムを主成分とするもの、Ｐｂ系ペロブスカイト酸化物を主成分とするものが主として考えられるが、他の系の誘電材料でも構わない。

【００６５】電極としては、高周波特性及び高信頼性を重視する場合は、Ａｕ電極が用いられるが、これに限定されるものではなくＡｇメタライズ電極、Ｎｉ電極他いずれでも用途に応じて用いればよい。なお、Ａｕ電極を用いる場合は、下地の電極としてＴｉＷが保護膜として好ましい。

【００６６】一方、層間ビア接続を実現するための前記貫通孔の形成方法は、前記シート状基材の種類等により

適宜決定されるが、例えば、炭酸ガスレーザー加工、パンチングマシーンによる加工、金型による一括加工等があげられる。

【００６７】前記導電性ペーストとしては、導電性を有していれば、特に制限されないが、通常、導電性金属材料の粒子を含有する樹脂等が使用できる。前記導電性金属材料としては、例えば、銅、銀、金、銀パラジウム等が使用でき、前記樹脂としては、エポキシ系樹脂、フェノール系樹脂、セルロース系樹脂、アクリル系樹脂等の有機バインダーが使用できる。

【００６８】なお、本実施形態では、導電性ペースト充填による層間接続を想定しているが、スルーホールメッキビアによる接続構造であっても何ら構わない。

【００６９】（実施の形態２）つぎに、本発明の第２の実施の形態であるチップ部品内蔵多層基板を図３に示す。基板３０１に内蔵されたチップ部品３０４が単層チップコンデンサであり、上面には、一極電極３０５が、下面には、多数の電極３０６が形成されていて、これら面内に収まる一極電極である外部接続電極３０５と前記電気絶縁性多層配線基板３０１に形成された配線パターン３０３とが接続され、多数電極である外部接続端子３０６と前記電気絶縁性多層配線基板３０１に形成された層間接続ビア３０２とが、ランド配線層３０７を介して接続された構成である。下面に形成された多数電極３０６は、図３に示すようにグリッド状の形態をとって、多端子構造をとってもよい。

【００７０】このような構造によれば、実装形態によって設計値どおりの静電容量を示さないコンデンサに対し、異なる複数個のチップコンデンサを用意することができるので、必要とされる静電容量を容易に提供することができる。これは、内蔵に伴う容量変化が生じた場合に特に、有効に機能する。

【００７１】（実施の形態３）次に、本発明の第３の実施形態であるチップ部品内蔵多層基板の構成概略を図４に示す。図４において、チップ部品４０４が、セラミックスからなる複数の誘電体層４０６と該誘電体層の内部に形成される内部電極４０４及び内部電極と上面あるいは下面に形成された外部端子電極が電気的に接続するように前記誘電体層を貫通するビアホール接続部４０２を備えたチップ積層コンデンサ４０４が基板４０１に埋設されたものである。なお、層間の接続はビアホール接続部４０７にて行われる。従って、下面電極のみ（埋め込み後は上面電極）で接続端子を取り出すことができる点、及び従来の外部端子電極が、側面電極で構成されている積層チップコンデンサの場合と比較して、本実施形態のチップコンデンサでは、外部端子電極と内部積層電極との距離が短い構造となるため、浮遊容量を小さくすることができ、正確な容量を導出することができる。

【００７２】（実施の形態４）次に、本発明の第４の実施形態であるチップ部品内蔵多層基板の構成概略を図５に示す。図５において、セラミック焼結体５０５の下面と垂直な方向に沿ってセラミック層を介して重なり合うように配置された複数の内部電極５０６とを備え、複数の内部電極は、静電容量を取り出すために、その端円の一部がセラミック焼結体の上面及び下面に露出されており、前記セラミック焼結体の上面に形成された第一の外部電極５０７と、セラミック焼結体の下面に形成された少なくとも１つの第２の外部電極５０８とをさらに備え、基板５０１に埋設された構造であり、基板５０１内に形成された層間接続ビア５０２と外部電極５０８とが配線層５０４を介して接続されている。さらに、チップコンデンサ上両面電極５０７と、配線層５０３とが接続して配置されている。

【００７３】この構造によれば、積層構造を採用しているため、チップコンデンサとして大容量の静電容量を取り出すことができる。また、ビアホール接続部を用いずに上下面に端子電極を構成することができるため、容易にチップコンデンサを作製することができる。従って、大容量のコンデンサで且つ、厚みの伴わないチップコンデンサ内蔵基板を得ることができる。

【００７４】また、本発明では、チップ部品の代表としてチップコンデンサを各実施形態、実施例でも採用しているが、積層セラミックインダクター、チップ抵抗等を採用しても有効であることは言うまでもない。

【００７５】この積層コンデンサは、直方体のセラミック焼結体を用いて構成されており、例えばチタン酸バリウム系セラミックのような適宜の誘電体セラミックを用いることができる。

【００７６】セラミック焼結体には、複数の内部電極がセラミック層を介して重なり合うように配置されている。

【００７７】（実施の形態５）つぎに、本発明の第５の実施の形態であるチップ部品内蔵多層基板を図６に示す。基板６０１に内蔵されたチップ部品６０４が積層チップコンデンサであり、実施の形態４と同様に、セラミック焼結体６０５の下面と垂直な方向に沿ってセラミック層を介して重なり合うように配置された複数の内部電極６０６とを備え、複数の内部電極は、静電容量を取り出すために、その端円の一部がセラミック焼結体の上面及び下面に露出されており、前記セラミック焼結体の上面に形成された複数の外部電極６０７と、セラミック焼結体の下面に形成された複数の外部電極６０８とをさらに備え、基板６０１に埋設された構造であり、基板６０１内に形成された層間接続ビア６０２あるいは配線層６０３が外部複数電極６０７あるいは６０８に接続されている。前記複数電極６０７，６０８は、図３に示すようにグリッド状の形態をとって、多端子構造をとってもよい。

【００７８】（実施の形態６）つぎに、本発明の第６の実施の形態であるチップ部品内蔵多層基板を図７に示

す。図7は実施の形態4と同様、セラミック焼結体705の下面と垂直な方向に沿ってセラミック層を介して重なり合うように配置された複数の内部電極706とを備え、複数の内部電極は、静電容量を取り出すために、その端円の一部がセラミック焼結体705の上面及び下面に露出されており、前記セラミック焼結体の上面に形成された第一の外部電極707と、セラミック焼結体の下面に形成された少なくとも1つの第2の外部電極708とをさらに備え、基板701に埋設された構造であり、基板701内に形成された配線形成層703と外部電極708とが導電性接着剤で接続、実装されたものである。従って、半田フリーの実装形態であるため、前記セラミック焼結体705に非鉛系材料のチップ部品を採用すれば、完全に非鉛系材料で構成されたチップ部品内蔵基板を作製することができる。

【0079】なお、内蔵されるチップ部品は、なんら図7に示す積層構造のチップコンデンサに限定されるものではなく、単層チップコンデンサでもよく、またチップインダクター、チップ抵抗でも構わない。

【0080】（実施の形態7）つぎに、本発明の第7の実施の形態であるチップ部品内蔵多層基板を図8に示す。図8は実施形態6と同様、縦型電極の積層構造のチップコンデンサ804が基板801に埋設され、基板801内に形成された接続ビア802と前記チップコンデンサ804の外部接続電極806とが接続された構造であり、且つ前記内蔵チップコンデンサ804と前記基板の表層に実装された半導体素子808とがデカップリングをしている構造であるため、半導体素子808とチップコンデンサ804との最短距離実装が実現されており、低ノイズ化等の優れた特性を有するデバイスを実現することができる。

【0081】なお、内蔵されるチップ部品は、なんら図8に示す積層構造のチップコンデンサに限定されるものではなく、単層チップコンデンサでも構わない。

【0082】（実施の形態8）つぎに、本発明の第8の実施の形態であるチップ部品内蔵多層基板を図9に示す。図9は実施形態7と同様、縦型電極の積層構造のチップコンデンサ904が基板901に埋設され、基板901（a）内に形成された接続ビア902と前記チップコンデンサ904の外部接続電極906とが接続された構造と半導体素子908が基板901（b）に内蔵された構造とが積層されたものであり、チップコンデンサ内蔵配線層904と前記半導体素子が内蔵された配線層905とが層間ビア902を介して接続され、チップコンデンサ904と半導体素子908とがデカップリングをおこなう構造であるため、半導体素子とチップコンデンサとの最短距離実装の実現及び最大限の体積効率化が実現された、積層内蔵基板全体の薄型化を実現することができる。

【0083】なお、内蔵されるチップ部品は、なんら図9に示す積層構造のチップコンデンサに限定されるものではなく、単層チップコンデンサでも構わない。

【0084】（実施の形態9）同様に、本発明の第9の実施の形態であるチップ部品内蔵多層基板を図10に示す。図10は上記実施形態8と同様、縦型電極の積層構造のチップコンデンサ1004が基板1001に埋設され、基板1001内に形成された層間接続ビア1002と前記チップコンデンサ1004の外部接続電極1006とが接続された構造は同様であるが、同一基板1001内に同じく半導体素子1008が内蔵され、前記基板1001に形成された配線層1005とがフリップチップ接続しており、さらに層間ビア1002と前記配線層1005を介してチップコンデンサ1004と半導体素子1008とがデカップリングをおこなう構造である。この構造によれば、チップコンデンサ1004を内蔵する工程と半導体素子1008を内蔵する工程を同時に行うことができるため、工程を簡略化でき、且つ半導体素子とチップコンデンサとの最短距離実装の実現及び最大限の体積効率化が実現できる。

【0085】なお、内蔵されるチップ部品は、なんら図10に示す積層構造のチップコンデンサに限定されるものではなく、単層チップコンデンサあるいは積層チップインダクター、チップ抵抗でも構わない。

【0086】一方、前記チップ部品や半導体素子を埋め込む基板としては、次のようなシート状基材が望ましい。例えば、前記シート状基材が無機フィラーと熱硬化性樹脂組成物とを含み、少なくとも一つの貫通孔を有し、前記貫通孔に導電性ペーストが充填されていることが好ましい。これにより、熱伝導性に優れ、前記配線パターンが前記導電性ペーストにより電気的に接続されたＩＶＨ構造を有する高密度実装用配線基板を容易に得ることができる。

【0087】また、このシート状基材を用いれば、配線基板の作製の際に、高温処理の必要がなく、例えば、熱硬化性樹脂の硬化温度である200℃程度の低温処理で十分である。

【0088】前記シート状基材全体に対し、前記無機フィラーの割合が70～95重量％であり、前記熱硬化性樹脂組成物の割合が5～30重量％であることが好ましく、特に好ましくは、前記無機フィラーの割合が85～90重量％であり、前記熱硬化性樹脂組成物の割合が10～15重量％である。前記シート状基材は、前記無機フィラーを高濃度含有できることから、その含有量により、配線基板における、熱膨張係数、熱伝導度、誘電率等を任意に設定することが可能である。

【0089】前記無機フィラーは、Al_2O_3、MgO、BN、AlNおよびSiO_2からなる群から選択された少なくとも一つの無機フィラーであることが好ましい。前記無機フィラーの種類を適宜決定することにより、例えば、熱伝導性、熱膨張性、誘電率を所望の条件に設定

することが可能であり、例えば、前記シート状基材における平面方向の熱膨張係数を、実装する半導体の熱膨張係数と同程度に設定し、かつ高熱伝導性を付与することも可能である。

【００９０】前記無機フィラーの中でも、例えば、Al_2O_3、ＢＮ、ＡｌＮ等を用いたシート状基材は、熱伝導性に優れ、ＭｇＯを用いたシート状基材は、熱伝導度に優れ、かつ熱膨張係数を大きくすることができる。またSiO_2、特に非晶質SiO_2を使用した場合、熱膨張係数が小さく、軽く、かつ低誘電率のシート状基材を得ることができる。なお、前記無機フィラーは、一種類でもよいし、二種類以上を併用してもよい。

【００９１】前記無機フィラーと熱硬化性樹脂組成物とを含むシート状基材は、例えば、以下のようにして作製できる。まず、前記無機フィラーと熱硬化性樹脂組成物とを含む混合物に粘度調整用溶媒を加え、任意のスラリー粘度であるスラリーを調製する。前記粘度調製用溶媒としては、例えば、メチルエチルケトン、トルエン等が使用できる。

【００９２】そして、予め準備した離型フィルム上において、前記スラリーを用いて、例えば、ドクターブレード法等により造膜し、前記熱硬化性樹脂の硬化温度よりも低い温度で処理して、前記粘度調整用溶媒を揮発させた後、前記離型フィルムを除去することによりシート状基材が作製できる。

【００９３】前記造膜した時の膜厚は、前記混合物の組成や、添加する前記粘度調整用溶媒の量により適宜決定されるが、通常、厚み８０～２００μｍの範囲である。また、前記粘度調製用溶媒を揮発させる条件は、例えば、前記粘度調製用溶媒の種類や前記熱硬化性樹脂の種類等により適宜決定されるが、通常、温度７０～１５０℃で、５～１５分間である。

【００９４】前記離型フィルムとしては、通常は、有機フィルムが使用でき、例えば、ポリエチレン、ポリエチレンフタレート、ポリエチレンナフタレート、ポリフェニレンサルファイド（ＰＰＳ）、ポリフェニレンフタレート、ポリイミドおよびポリアミドからなる群から選択された少なくとも一つの樹脂を含む有機フィルムであることが好ましく、特に好ましくはＰＰＳである。

【００９５】また、別のシート状基材としては、シート状補強材に熱硬化性樹脂組成物を含浸したものであり、少なくとも一つの貫通孔を有し、前記貫通孔に導電性ペーストが充填されているシート状基材がある。

【００９６】前記シート状補強材は、前記熱硬化性樹脂を保持できるものであれば、特に制限されないが、ガラス繊維の織布、ガラス繊維の不織布、耐熱有機繊維の織布および耐熱有機繊維の不織布からなる群から選択された少なくとも一つのシート状補強材であることが好ましい。前記耐熱有機繊維としては、例えば、全芳香族ポリアミド（アラミド樹脂）、全芳香族ポリエステル、ポリプチレンオキシド等があげられ、中でもアラミド樹脂が好ましい。

【００９７】前記熱硬化性樹脂は、耐熱性であれば特に制限されないが、特に耐熱性に優れることから、エポキシ系樹脂、フェノール系樹脂およびシアネート系樹脂あるいはポリフェニレンフタレート樹脂、ポリフェニレンエーテル樹脂からなる群から選択された少なくとも一つの樹脂を含むことが好ましい。また、前記熱硬化性樹脂は、いずれか一種類でもよいし、二種類以上を併用してもよい。

【００９８】このような、シート状基材は、例えば、前記熱硬化性樹脂組成物中に前記シート状補強材を浸漬した後、乾燥させ半硬化状態にすることにより作製できる。

【００９９】前記含浸は、前記シート状基材全体における前記熱硬化性樹脂の割合が、３０～６０重量％になるように行うことが好ましい。

【０１００】これらの製造方法において、以上のような、熱硬化性樹脂を含有するシート状基材を用いる場合は、前記配線基板の積層を、加熱加圧処理による前記熱硬化性樹脂の硬化によって行うことが好ましい。これによれば、前記配線基板の積層工程において、例えば、前記熱硬化性樹脂の硬化温度である２００℃程度の低温処理で十分である。

【０１０１】前記シート状補強材が、ポリイミド、ＬＣＰ、アラミドなどのフィルム上シートに熱硬化樹脂をコーティングしたものであってもよい。

【０１０２】（実施の形態１０）次に、本発明の第１０の実施の形態であるチップ部品内蔵多層基板の製造方法を従来の実施の形態である製造方法、図１１と比較しながら図１２に示す。

【０１０３】図１１(a)(b)のように、既に提案がなされている実施形態である転写用部品配線パターン形成材は、第一の金属層である離型キャリア用金属箔１１０６と、その上に形成された第二の金属層である配線用金属層１１０３の２層構造で形成された転写用配線パターン形成材上に、チップ部品接続用の半田ペースト１１０５が印刷される。なお、導電性接着剤を用いて転写用配線パターンとチップ部品を接続してもよい。

【０１０４】次に、図１１(c)のように、チップ部品１１０４を所定の位置にセットした後、リフロー炉を通過させて、チップ部品を転写形成材上に実装した。

【０１０５】しかる後、図１１（ｄ）～（ｅ）に示すように、層間接続ビア１１０２が形成された、基板を構成するシート状基材１１０１に、位置合わせを行いながら圧着を行い、チップ部品が実装された転写形成材を押しつけ、シート状基材の硬化も同時に行った。

【０１０６】その後、図１１（ｆ）に示すように、離型キャリア用金属箔１１０６部分のみをエッチングによって除去し、チップ部品１１０４が内蔵された基板が得ら

れる。

【0107】この場合、チップ部品は、寝かした状態で転写形成材に半田実装されているが、立てた状態で半田実装を行い、基板に埋め込む場合も従来例として報告されている。しかし、その場合は、チップ部品の長さ方向がそのまま層厚に対応して埋設されることが多く、その基板の層厚が厚くなり、多層化していくことが現実的に困難であった。

【0108】いずれにせよ、転写形成材の配線パターンとチップ部品の側面電極を安定して半田接続させるためには、ある一定以上の実装面積が必要になる。従って、チップ部品のごく近傍に配線を配置させることは困難となっており、高密度実装を妨げていた。

【0109】一方、本発明第10の実施の形態の製造方法では、上下両面に電極を有する単層チップコンデンサ1204を転写形成材に構成されている配線パターン1203上に実装することになるため、図12(e)に示すように半田実装または導電性接着剤によって実装する場合でも、実装面積は、チップ面積内あるいは、それと同等の面積で容易に行うことができる。

【0110】これらの製造方法によれば、ドライフィルムレジスト（DFR）を用いて逆パターンを形成した後、無電解メッキあるいは電解メッキを含むパターンメッキ法やスパッタリング法、蒸着法等の直接描画法を用いて配線パターン金属層を形成することから、微細な配線パターン形成することが可能である。また、配線パターンを構成する金属箔は、メッキ法の場合は、キャリアを構成する金属箔は、例えば銅箔と同一にしておくことも、また異なる金属である銀メッキ膜によって構成することもできる。また、前述と同様の理由から、第1の金属層であるキャリア用金属箔を再利用したりすることも可能であるため、低コスト化が可能であり、工業上の利用性にも優れる。

【0111】また、転写形成剤を用いて単層チップコンデンサを埋め込む際には、図12（f）に示すように、予め、チップコンデンサ接続用の配線パターンをシート状機材1201に転写しておいてから行ってもよいが、配線パターンによっては、直接、チップ部品1204と層間接続ビア1202が接続するように埋め込んでも構わない。

【0112】また、本実施の形態では、転写形成材を構成する離型キャリア銅箔1206は、エッチングではなく、離型キャリア1206のみを剥離して部品配線パターンの転写を実現させることができる事を確認している。

【0113】この製造方法によれば、チップ部品の実装に要する面積も少なく、また厚みも薄いため、部品内蔵層の厚みを100～200μm程度に抑制することができ、多層化していくことも十分可能となる。

【0114】（実施の形態11）つぎに、本発明の第11の実施の形態であるチップ部品内蔵多層基板の製造方法を図13に示す。

【0115】図13(a)～(c)に示すように、本実施の形態では、まず、離型樹脂フィルム1301上に粘着フィルム層1302を形成した後、配線パターン層1303を形成する。しかる後、実施形態10と同様に単層チップコンデンサ1304を転写形成材上に実装する。但し、本実施形態で用いられる単層チップコンデンサ1304は、片面のみ単一電極であり、もう片面は、多数の電極で構成されている。本実施の形態では、図13(g)～(i)に示すように、複数電極面側でチップ部品と転写配線パターンを実装接続した後、位置合わせを行いながらシート状機材1306に圧着、埋め込み工程を行っている。埋め込みにあたっては、図13(f)に示すように予め、もう片面側の配線パターンを転写しておいた。しかる後に、離型キャリア樹脂フィルムを手動で剥離した。本実施形態のように転写形成材の離型用フィルムに樹脂を用いると、転写形成材上に実装されたチップ部品の導通等を埋め込み前に予めチェックしておくことができる。

【0116】また、本実施形態のように単層チップコンデンサの外部端子電極を複数にしておくと所定の静電容量を容易に得ることができる。特に、基板内蔵に伴い静電容量が変化する場合に調整が容易であり、特に有効である。

【0117】なお、本実施形態の製造方法では、単層チップコンデンサを用いているが、図5，図6に示すような縦電極の積層チップコンデンサ、チップインダクター、チップ抵抗をもちいても何ら構わない。

【0118】（実施の形態12）つぎに、本発明の第12の実施の形態であるチップ部品内蔵多層基板の製造方法を図14に示す。図14に示すように、本実施形態に用いられる転写形成材は、第一の金属層である離型キャリア用金属箔1406と、その上に形成された剥離層1407と、さらにその上に形成された第二の金属層である配線用金属1403の3層構造で形成される。

【0119】これら前記転写用部品配線パターン形成材において、前記第1の金属層と配線層を構成する第2の金属層の接着強度が弱いこと、例えば50gf/cm以下であることが好ましい。前記第1の転写用部品配線パターン形成材では、メッキ法や蒸着法等を用いることにより、エッチング、メッキ、水洗等のプロセス下では、2層の金属層間が剥がれないが、ピールに際しては容易に第2の金属層のみ、剥離させることができることが認められている。また、半田あるいは導電性接着剤で形成されたチップ部品パターンは、容易に、キャリアである第1の金属層から剥離させることができる。

【0120】一方、前記転写用部品配線パターン形成材では、剥離層として接着力を有した1μmより薄い有機層、例えば熱硬化樹脂であるウレタン系樹脂、エポキシ

系樹脂、フェノール樹脂などが使用できるが、これには制限されず、他の熱可塑性樹脂などを用いても構わない。但し、1μmより厚くなると、剥離性能が悪化し、転写が困難となる場合があるので1μm以下が好ましい。

【0121】一方、意図的に接着力を低下させる目的で剥離層1407としてメッキ層を介在させても良い。例えば、1μmより薄い金属メッキ層、ニッケルメッキ層あるいはニッケルリン合金層あるいはアルミニウムメッキ層等を銅箔間に介在させて剥離性を持たせることも可能である。

【0122】これにより、前記第2の金属層からなる配線部に関しては、基板に転写する際に、前記第1の金属層から前記第2の金属層が剥離し易く、前記第2の金属層及び部品パターンを前記基板に転写することが容易になる。金属メッキ層の場合、剥離層は、100nmから1μmの厚みレベルで十分であり、厚くなればなるほど工程上コストがかかるので、少なくとも1μmより薄いことが望ましい。

【0123】前記転写用部品配線パターン形成材において、前記第1の金属層は、銅、アルミ、銀およびニッケルからなる群から選択された少なくとも一つの金属を含むことが好ましいが、中でも銅を含むことが好ましい。前記第2の金属層は、第1の金属層と同様、銅、アルミ、銀およびニッケルからなる群から選択された少なくとも一つの金属を含むことが好ましいが、前記第1の転写用部品配線パターン形成材の場合は銀を、前記第2あるいは第3の転写用部品配線パターン形成材の場合は、銅を含むことが好ましい。なぜなら、第1の金属層に銅を用いるの場合は、コスト的に安いこと、つまり、市販のもので所定の厚みを有する箔が多く存在することためである。また、第2の金属層に銅を用いる場合は、メッキで生成することが容易であるためである。また、第3の実施形態での転写形成材の場合、第1の金属層と第2の金属層が同一であれば、同じエッチング液で加工を制御できるという効果があるが、金属層が銅の場合は、エッチングによるファインな加工条件だしが既に良く開発されているという利点がある。なお、前記金属は、一種類でもよいが、二種類以上を併用してもよい。

【0124】前記第1および第2および第3の転写用部品配線パターン形成材において、前記第2の金属層の厚みが、1～18μmの範囲であることが好ましく、特に好ましくは、3～12μmの範囲である。前記厚みが3μmより薄いと、前記第2の金属層を基板に転写した場合に、良好な導電性を示さないおそれがあり、前記厚みが18μmより厚いと、微細な配線パターンを形成することが困難となるおそれがある。

【0125】前記転写用部品配線パターン形成材において、前記第1の金属層の厚みが、4～100μmの範囲であることが好ましく、特に好ましくは、20～70μmの範囲である。第1の金属層は、キャリアとして機能する一方、場合によっては本実施形態に示すように、配線層と同様に表層部がエッチングされて凹凸を有する構造となるため、十分な厚みを有した金属層であることが望ましい。また、転写用に用いるキャリア層を金属層とすることで、転写時に生じる熱歪みや、平面方向の応力歪みに対して十分な機械強度や耐熱性を示す。

【0126】配線パターン形成するための化学エッチングは具体的には次のように行うことができる。アンモニウムイオンを含む塩基性塩化第2銅水溶液をエッチャントに用いると、剥離層が例えばニッケルリン合金層からなる場合は、第2の金属層のみをエッチングすることができる。しかる後に、エッチング液に硝酸、過酸化水素水の混合液を用いると、剥離層のみを取り除くことができる。転写後に配線部が凹部にならず、平坦になるように意図する場合に用いられる。

【0127】また、配線パターンを構成する金属箔をキャリアを構成する金属箔と同一にしておくことによって、本実施形態のように一回のエッチングプロセスでキャリアを構成する第1の金属層まで配線パターンと同一の凹凸形状を形成することができる。

【0128】また、転写を行った後の、前記第2の金属層以外の転写用配線パターン形成材の構成材料を再利用したり、特に後者の場合は、配線パターン状に加工されていることを利用して凸版印刷として違うやり方のパターン形成に利用することも可能である。このため、低コスト化が可能であり工業上の利用性にも優れる。

【0129】なお、これら前記転写用部品配線パターンの構成において、第2の配線パターン上に電解メッキ法により前記第2の金属層上に前記金属層を形成してもよい。前記電解メッキ法により第3の金属層、または前記配線パターン形成用の金属層を形成すれば、前記第2の金属層と前記第3の金属層との接着面に適度な接着性が得られるだけでなく、前記金属層間に隙間が発生しないため、例えばエッチング等を行っても良好な配線パターンを形成できる。一方、第2の金属層上に前記第3の金属層をパネルメッキで形成した後、配線パターン上にマスキングを行いパターン形成を行ってもよい。この場合、転写後の第2の金属層の表面酸化防止、ハンダ濡れ性の改善に効果がある。

【0130】この転写用配線パターンの製造方法において、前記第2の金属層上に第3の金属層を形成する前には、前記第2の金属層の表面を粗面化処理することが好ましい。前記金属層を形成する前とは、前記第2の金属層上に配線パターン用の金属層を形成する前、または前記配線パターン状にマスキングされた第2の金属層上に、前記配線パターンに沿って第2の金属層を形成する前をいう。このように、前記第2の金属層を粗面化処理すると、前記第2の金属層と前記第3の金属層との接着性が向上する。

【０１３１】さらに、前記転写用配線パターンの製造方法において、電解メッキ法により前記第３の金属層上に異なる金属層を形成してもよい。前記電解メッキ法により異なる金属層、すなわち、前記第１から第３の金属層を腐食するエッチング液に対し化学的に安定な金属成分を選択することにより、前記転写用配線パターンの製造方法において、化学エッチング法により、何ら第２，３，４の金属層の厚みを低減させることなく、前記第１の金属層の表層部を含めて配線パターン状に加工することができるため好ましい。

【０１３２】この異なる金属で構成された層としては、例えば、化学的に安定で低抵抗なＡｇ、あるいはＡｕメッキ層などが望ましい。これらは酸化されにくい金属であるため、これらでメッキされた配線層と例えば、予め基板に形成されたビアあるいは、ベアチップのバンプや導電性接着剤との接続性などはより安定させることができる。

【０１３３】一方、チップ部品及び配線パターンが表層に転写される場合は、特にインダクタ、コンデンサ、半導体チップ等の端子間距離が接近している場合などは、沿面距離をかせぐ意味からも、本実施形態のように、キャリア層１４０６まで部分的に加工された転写形成材が好ましい。

【０１３４】また、配線部分がこのように凹形状である場合は、例えば、半導体のフリップチップ実装等行う場合に優れた実装性を発揮する。

【０１３５】（実施の形態１３）同様に、つぎに、本発明の第１３の実施の形態であるチップ部品内蔵多層基板の製造方法を図１５に示す。本実施形態は、部品内蔵層が二層以上の多層に積層されたことを特徴とする。

【０１３６】図１５(a)に示すように、前記実施形態同様の配線パターン１５０３が形成された転写形成材上に半導体ベアチップ１５１０をフリップチップ実装する。１５０９は実装を補強するためのアンダーフィルである。また、本実施形態では、同時に印刷によって形成された抵抗体１５１１も加えた。

【０１３７】前記回路基板は、１００℃以下の低温で部品パターン及び配線パターンを転写形成ができるので、熱硬化樹脂を用いたシートに於いても、未硬化の状態を維持することができ、図１５（ｄ）に示すように一括積層による熱硬化収縮を実現することができる。

【０１３８】従って、４層以上の多層を有する回路基板に於いて、各層毎の硬化収縮の補正を行う必要がない。これにより、微細な配線パターン及び部品パターンを有する多層構造の回路基板を作製できる。但し、内層を形成する配線部、部品部に関しては、前述のように凹形状である必要はなく平坦でもよい。

【０１３９】また、図１５（ｄ）（ｅ）に示すように、本実施形態のように多層回路基板を作製する場合は、前述のようにして作製した半導体素子、あるいはチップ部品等が内蔵されたそれぞれの単層の回路基板を積層し、層間を接着することにより作製できる。当然ながら、本実施形態のようにＢステージの配線パターンと層間ビアが形成された配線層１５１２，１５１３を付け加えて、一括で５層板に積層することができる。

【０１４０】また、この構造によれば、半導体素子とパスコンとして機能するチップコンデンサをごく近傍に位置するように実装できるので、優れた特性を見いだすことができる。

【０１４１】なお、本実施形態に示したように、内蔵する部品は、チップ部品に限定するものではなく、半導体素子、さらには印刷等によって作製された膜状のＬＣＲ各種部品も内蔵させることができる。

【０１４２】例えば、シート状基材が熱硬化性樹脂を含む回路基板を積層する場合は、図１５(ｄ)～(e)に示すように、まず、前述と同様に、加熱加圧処理によって、前記シート状基材に熱硬化しない低温域で前記部品配線パターンのみを転写し、得られた単層の回路基板を積層する。そして、前記積層体を、前記熱硬化性樹脂の硬化温度で加熱加圧処理し、前記熱硬化性樹脂を硬化することによって、前記回路基板間を接着固定する。加熱加圧条件の温度を意図的に１００℃以下にして回路層の転写を行うと、転写後もシート状基材を殆どプリプレグのように扱えるため、順次積層でない一括積層による多層化が可能となる。

【０１４３】前記多層回路基板における積層数は特に制限されないが、通常、４～８層であり、１２層に及ぶものもある。また、前記多層回路基板の全体の厚みは、通常、５００～１０００μｍである。

【０１４４】なお、前記多層回路基板の最外層以外の中間層を構成する回路基板は、インナービアによる電気的接続構造を考慮すると、配線パターン等が表面に埋め込まれた凹部ではなく、平坦であってもよい。この構造を意図的に得るためには、本願発明の第１あるいは第２の転写用部品配線パターンを用いるとよい。また、前記多層構造の最外層は前記表面が平坦な構造の回路基板でもよいが、表面に凹部を有しその底部に第２の金属層等が形成された配線基板であると、半導体チップ等の実装がより容易になり好ましい。

【０１４５】（実施の形態１４）同様に、つぎに、本発明の第１４の実施の形態であるチップ部品内蔵多層基板の製造方法を図１６に示す。本実施形態は、実施形態１３と同様に、部品内蔵層が二層以上の多層に積層されたことを特徴とする。

【０１４６】本実施形態の製造方法によれば、個々の半導体素子、チップ部品を内蔵する工程は、実施形態１３と同様であるが、内蔵工程と同時に回路基板であるシート状基材を完全に硬化してしまうところが異なる。この製造方法によれば、各部品内蔵層１６０１，１６０２は完全に硬化しているため、積層の層間接続にあたって

は、接着材の役割を果たすBステージの配線層１６０３を介して行うことになる。

【０１４７】従って、積層工程に於いては、既に半導体素子１６１０、チップ部品１６１１等の部品は、硬化した基板１６０１，１６０２で守られているため、損傷を受ける可能性がより少なくすることができる。

【０１４８】（実施の形態１５）つぎに、本発明の第１５の実施の形態であるチップ部品内蔵多層基板の製造方法を図１７に示す。本実施形態は、同一部品内蔵層にチップ部品及び半導体素子が内蔵されており、且つチップ部品と半導体素子とがごく近傍に位置して接続された構造を特徴とする。

【０１４９】本実施形態の製造方法によれば、個々の半導体素子、チップ部品を内蔵する工程に転写形成材を用いる点は前記実施形態と同じであるが、それぞれのチップ部品を含む転写形成材１７１０及び半導体素子１７０５を含む転写形成材１７０６を同時に回路基板であるシート状基材の上下両面から埋め込み、内蔵を行うところが特徴である。この製造方法によれば、各部品内蔵層は１層でありながら、半導体素子１７０３が層間接続ビア１７０８を通じてチップ部品１７０４と短配線で接続された構造を実現することができる。

【０１５０】この場合、チップ部品１７０４がバスコンであれば、ＭＰＵ等の半導体素子とデカップリングを行い、優れた機能を発揮することができる。

【０１５１】

【実施例】つぎに、実施例を用いて、図に基づき、本発明をさらに具体的に説明する。

【０１５２】（実施例１）図１２は、前記転写用配線パターン形成材の製造工程の概略の一例を示す断面図である。図１２（ａ）に示すように、第１の金属層１２０６として、厚み３５μｍの電解銅箔を準備した。まず、銅塩原料をアルカリ性浴に溶解し、これを高電流密度となるように回転ドラムに電着させ、金属層（銅層）を形成し、この銅層を連続的に巻き取って、電解銅箔を作製した。

【０１５３】つぎに、図１２（ｂ）に示すように、ドライフィルムレジスト１２０９を用いて、配線逆パターンを形成した。しかる後に、図１２（ｃ）に示すように、前記第１の金属層１２０６の面上に、銀で構成された配線パターン形成用の金属層１２０３を、厚み９μｍになるように、電解メッキ法によって積層し、図１２（ｄ）に示すように、２層構造からなる転写用配線パターン形成材を作製した。この表面の中心線平均粗さ（Ｒａ）が、４μｍ程度になるように粗面化処理を施した。

【０１５４】次に、単層チップコンデンサの実装位置に半田ペーストを用いて印刷した後、前記コンデンサを装着し、リフロー炉にて接続を確保した。

【０１５５】まず、配線パターンを転写する基板１２０１を準備した。この基板１２０１は、コンポジット材料からなるシート状基材を調製し、これにビアホールを設け、前記ビアホールに導電性ペースト１２０７を充填することにより作製した。以下に、前記シート状基板１２０１の成分組成を示す。

【０１５６】（シート状基板１２０１の成分組成）

(1)Al_2O_3（昭和電工社製、ＡＳ－４０：粒径１２μｍ）：９０重量％

(2)液状エポキシ樹脂（日本レック社製、ＥＦ－４５０）：９．５重量％

(3)カーボンブラック（東洋カーボン社製）：０．２重量％

(4)カップリング剤（味の素社製、チタネート系：４６Ｂ）：０．３重量％

前記各成分を、前記組成になるように秤量して、これらの混合物に、粘度調整用溶剤としてメチルエチルケトン溶剤を、前記混合物のスラリー粘度が約２０Ｐａ・ｓになるまで添加した。そして、これにアルミナの玉石を加え、ポット中で４８時間、速度５００ｒｐｍの条件で回転混合し、スラリーを調製した。

【０１５７】つぎに、離型フィルムとして、厚み７５μｍのポリエチレンテレフタレート（ＰＥＴ）フィルムを準備し、このＰＥＴフィルム上において、前記スラリーを用いて、ドクターブレード法により、ギャップ約０．７ｍｍに造膜し、造膜シートを作製した。そして、この造膜シートを、温度１００℃で１時間放置することにより、前記シート中の前記メチルエチルケトン溶剤を揮発させ、前記ＰＥＴフィルムを除去し、厚み２００μｍのシート状基材１２０１を作製した。前記溶剤の除去を、温度１００℃で行ったため、前記エポキシ樹脂は、未硬化状態のままであり、前記シート状基材は可撓性を有していた。

【０１５８】このシート状基材を、その可撓性を利用して、所定の大きさにカットし、炭酸ガスレーザを用いて、ピッチが０．２ｍｍ～２ｍｍの等間隔になる位置に、直径０．１５ｍｍの貫通孔（ビアホール）を設けた。そして、この貫通孔に、ビアホール充填用導電性ペースト１２０７を、スクリーン印刷法により充填し、前記基板を作製した。前記導電性ペースト１２０７は、以下の材料を、以下の組成になるように調製し、三本ロールにより混練したものを用いた。

【０１５９】（導電性ペースト１２０２）

(1)球形状の銅粒子（三井金属鉱業社製：粒径２μｍ）：８５重量％

(2)ビスフェノールＡ型エポキシ樹脂（油化シェルエポキシ社製、エピコート８２８）：３重量％

(3)グルシジルエステル系エポキシ樹脂（東都化成社製、ＹＤ－１７１）：９重量％

(4)アミンアダクト硬化剤（味の素社製、ＭＹ－２４）：３重量％

つぎに、図１２（ｇ）に示すように、前記基板１２０１

の両面に、前記転写用部品配線パターン形成材のチップ部品パターン側が接するように配置し、熱プレスを用いて、プレス温度１２０℃、圧力１０kg/cm²で５分間、加熱加圧処理した。なお、コンデンサ１２０４に関して、上下電極面で挟む構造にする場合は、基板１２０１上に予め、電極パターン１２０７を転写形成しておいてもよい。

【０１６０】この加熱加圧処理により、前記基板１２０１中のエポキシ樹脂（前記シート状基材および導電性ペースト１２０２中のエポキシ樹脂）が溶融軟化して、図１２（ｇ）に示すように、前記チップ部品パターン１２０４および配線パターン１２０３が前記基板１２０１中に埋没した。そして、加熱温度をさらに上昇させ、温度１７５℃で６０分間処理することにより、前記エポキシ樹脂を硬化させた。

【０１６１】これにより、前記シート状基材と全部品パターンが、強固に接着し、また、前記導電性ペースト１２０２と各部品パターンとが電気的に接続（インナービア接続）し、かつ強固に接着した。

【０１６２】このような図１２（ｇ）に示す積層工程から、前記キャリア層である第１の金属層１２０６を剥離することにより、図１２（ｈ）に示すような、チップコンデンサ内蔵基板が得られた。

【０１６３】チップ部品の実装位置も、正確であり、厳密な設計どうりの回路基板を、容易に形成することができた。本実施例のチップコンデンサを含む転写形成材を用いた製造方法によれば、チップ部品と層間接続ビア１２０２と配線パターン１２０３との配線の接合は良好であり、良好に機能した。また、コンデンサ高温負荷信頼性試験（１２５℃、５０Ｖ、１０００時間）を行っても、コンデンサ１２０４の誘電体層に絶縁抵抗の劣化はなく、$10^6\Omega$以上の絶縁抵抗を確保できた。

【０１６４】この配線基板は、転写および加熱　　工程後、平坦な実装表面が形成された。本実施例では、この回路基板の配線層１２０３上に金メッキ層を形成してもよい。

【０１６５】この回路基板は、部品内蔵基板層の厚みが２００μmと比較的厚くない形態でチップ部品の内蔵を実現しており、且つ、基板の反り、クラック、ゆがみは、発生しなかった。

【０１６６】なお、本実施例では、基板の無機フィラーにアルミナ粉末を用いているが、酸化珪素粉末を用いても構わない。その場合、同様に通常のＦＲ－４等の樹脂基板と比較して高熱伝導性は維持されており、且つ、低誘電率３．５という特徴を見いだすことができた。

【０１６７】また、本実施例では、転写形成材にキャリア銅箔を用いているが、樹脂フィルムをキャリアとする転写形成材を用いても何ら構わない。

【０１６８】（実施例２）図１７(a)～(d)は、チップ部品を実装する前記転写用配線パターン形成材の製造工程の概略の一例を示す断面図である。

【０１６９】図１７（ａ）に示すように、第１の金属層１７０１として、厚み３５μmの電解銅箔を準備した。具体的には、銅塩原料をアルカリ性浴に溶解し、これを高電流密度となるように回転ドラムに電着させ、金属層（銅層）を作製し、この銅層を連続的に巻き取って、電解銅箔を作製した。

【０１７０】つぎに、図１７（ｂ）に示すように、前記第１の金属層１７０１の面上に、ニッケルリン合金で構成された薄いメッキ層を形成し、剥離層１７０２を形成する。配線パターン形成用の金属層１７０３として、前記第１の金属層１７０１と同じ電解銅箔を、厚み９μmになるように、電解メッキ法によって積層し、３層構造からなる積層体を作製した。

【０１７１】この表面の中心線平均粗さ（Ｒａ）が、４μm程度になるように粗面化処理を施した。なお、前記粗面化処理は、前記電解銅箔に、銅の微細な粒を析出させることにより、行った。

【０１７２】次に、化学エッチング法（塩化第２鉄水溶液に浸積）によりエッチングして、任意の配線パターンである第２の金属層１７０３および第１の金属層１７０１の表層部にパターニングを行った。

【０１７３】しかる後に、マスク部分を剥離剤で除去し、図１４（ｄ）に示す転写用配線パターン形成材を得た。第１の金属層と第２の金属層が同じ銅で構成されているため、一回の化学エッチングで第２の金属層のみならず第１の金属層にも部分的に凸部の配線層を形成することができる。キャリア層である第１の金属層まで一部加工されているところに構造上の特徴がある。なお、本実施例では、剥離層にニッケルメッキ層を用いているが、例えば、有機層等を形成しても、同様の構造を有する転写形成材を得ることができる。

【０１７４】この段階において作製された前記転写用配線のみのパターン形成材では、前記第１の金属層１７０１と配線パターン形成用の金属層１７０３との剥離層を介した接着性が接着力自体は弱くとも耐薬品性に優れ、この３層構造の金属層全体にエッチング処理を行っても、剥離することなく問題なく配線パターンを形成できた。一方、前記第１の金属層１７０１と第２の金属層１７０３との接着強度は、４０ｇ／ｃｍであり、剥離性に優れていた。

【０１７５】次に、内部に複数の縦電極を有する積層セラミックチップコンデンサ１７０４を導電性接着剤を用いて接続した。本構造のチップ積層コンデンサ１７０４は、上下面に外部接続端子があるため、容易に転写形成材上で実装することができた。

【０１７６】同様に、半導体素子１７０５も転写形成材上にフリップチップ実装を行い、図１７（ｄ）に示すように、基板内に形成されている層間接続ビア１７０８と位置合わせを行いながらシート機材に１５０℃加熱しな

がら押しつけた。本実施例に用いたシート基材は、実施例1と同様で、埋め込むためのプレス条件も同様である。

【0177】チップ部品を内蔵する工程に転写形成材を用いる点は前記実施例と同じであるが、それぞれのチップ部品を含む転写形成材及び半導体素子1705を含む転写形成材1706を同時に回路基板であるシート状基材の上下両面から埋め込み、内蔵を行うところが特徴である。

【0178】この製造方法によれば、各部品内蔵層は1層でありながら、半導体素子1705が層間接続ビア1708を通じてチップ部品1704と短配線で接続された構造を実現することができた。

【0179】この結果、パスコンであるチップ部品1704がMPU半導体素子1703とデカップリングを行い、高周波での優れた機能を発揮することができた。

【0180】また、回路基板を構成するシート状基材1707へ第2の金属層1703の転写を行った結果、前記第1の金属層1701と第2の金属層1703との剥離層を介した接着面が容易に剥離し、前記第2の金属層1703のみを前記基板に転写することができた。

【0181】この配線基板1707には、前記第1の金属層1701がエッチングされた深さに対応した凹部が形成され、前記凹部の底部に前記全ての配線を含む部品パターンが形成された。従って、この凹部の配線層が形成された表層にさらに他の半導体ベアチップをフリップチップしたところ、優れた実装性、信頼性を得ることができた。

【0182】チップ部品それぞれの実装位置も、正確であり、厳密な設計どうりの回路基板を、一括転写で形成することができた。本実施例の転写形成材によれば、半導体チップのバンプと配線の接合は良好であり、半導体チップのバイパスコンデンサとして機能するように実装したコンデンサも良好に機能した。また、コンデンサ高温負荷信頼性試験（125℃、50V、1000時間）を行っても、コンデンサの誘電体層に絶縁抵抗の劣化はなく、$10^6\Omega$以上の絶縁抵抗を確保できた。

【0183】

【発明の効果】以上のように、本発明のチップ部品内蔵基板は、微細な配線パターンの形成に加え、LCR等のチップ部品を半田あるいは導電性接着剤で実装、形成し、それらを一括して転写を行い内蔵化するため、容易に基板上に正確に実装することが可能である。また、内蔵に適したチップ部品を構成することにより、厳密な特性スペックの得られたチップ特性を内蔵後も生かすことができる点、内蔵してもチップ厚みが薄いため、層厚がかさばらないこと、上下面に電極を有するため、実装が容易で実装面積も不必要とすることができる。

【図面の簡単な説明】

【図1】(a)(b)は従来の実施の形態におけるチップ部品内蔵基板の構成概略を示す断面図

【図2】本発明の第1の実施の形態における部品内蔵基板の構成概略を示す断面図

【図3】本発明の第2の実施の形態における部品内蔵基板の構成概略を示す断面図

【図4】本発明の第3の実施の形態における部品内蔵基板の構成概略を示す断面図

【図5】本発明の第4の実施の形態における部品内蔵基板の構成概略を示す断面図

【図6】本発明の第5の実施の形態における部品内蔵基板の構成概略を示す断面図

【図7】本発明の第6の実施の形態における部品内蔵基板の構成概略を示す断面図

【図8】本発明の第7の実施の形態における部品内蔵基板の構成概略を示す断面図

【図9】本発明の第8の実施の形態における部品内蔵基板の構成概略を示す断面図

【図10】本発明の第9の実施の形態における部品内蔵基板の構成概略を示す断面図

【図11】（a）～（f）は、従来の転写用部品配線パターン形成材を用いて形成された多層回路基板の各層の製造工程の概略を示す断面図

【図12】（a）～（i）は、本発明の第10の実施の形態および実施例1における転写用チップ部品配線パターン形成材及びそれを用いて形成されたチップ部品内蔵基板の製造工程の概略を示す断面図

【図13】（a）～（i）は、本発明の第11の実施の形態における転写用部品配線パターン形成材及びそれを用いて形成されたチップ部品内蔵基板の製造工程の概略を示す断面図

【図14】（a）～（i）は、本発明の第12の実施の形態における転写用部品配線パターン形成材及びそれを用いて形成されたチップ部品内蔵基板の製造工程の概略を示す断面図

【図15】（a）～（e）は、本発明の第13の実施の形態におけるチップ部品内蔵基板の各層の製造工程の概略及び積層方法を示す断面図

【図16】（a）～（b）は、本発明の第14の実施の形態におけるチップ部品内蔵基板の各層の積層方法を示す断面図

【図17】（a）～（h）は、本発明の第15の実施の形態及び本発明の実施例2における転写用部品配線パターン形成材及びそれを用いて形成されたチップ部品内蔵基板の製造工程の概略を示す断面図

【符号の説明】

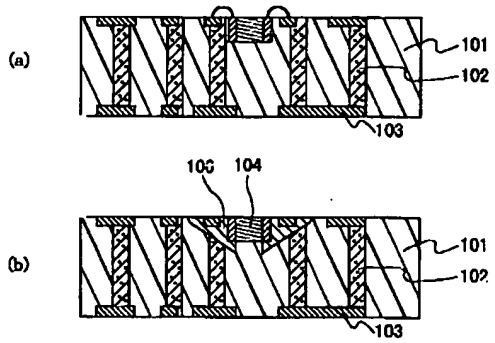
1106, 1206, 1301, 1406, 1504, 1701　キャリアを構成する第1の金属層

1208, 1302, 1407　剥離層

103, 203, 303, 403, 503, 603, 703, 803, 903, 1003, 1103, 1203, 1303, 1403, 1503, 1612, 1703　配線パターンを形成する

第2の金属層
101,201,301,401,501,601,701,801,901,1001,1101,1201,1306,1401,1501,1605,1706　シート状基材
102,202,302,402,502,602,702,802,902,1002,1102,1202,1307,1402,1502,1708導電性ペースト
104,1104　通常のチップ部品
204,304,1204,1304,1505,1617　単層チップコンデンサ
1404　層間接続ビアを有する積層コンデンサ
407　層間接続ビア
404　内層積層電極（平面方向）
403　外部接続端子
1704　縦積層内部電極を有する積層コンデンサ
506　内層積層電極（縦方向）
305,306,403,507,508,605,608,707,1205　外部接続端子電極
206,504,608,707,906,1006,1207　内蔵チップ部品と層間接続ビアをつなぐ配線層
1510,1610,1705　半導体チップ
1509,1609　アンダーフィル

【図1】



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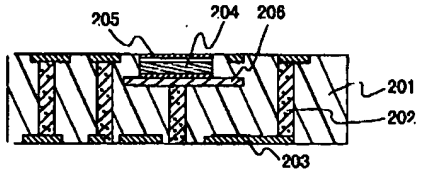

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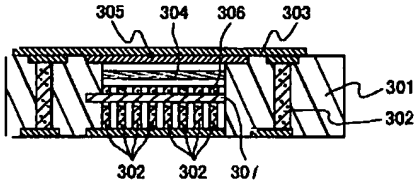

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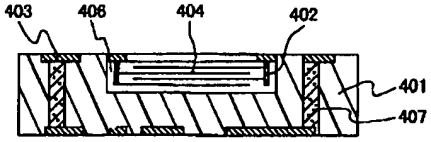

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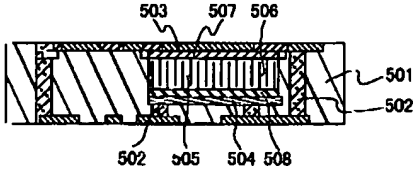

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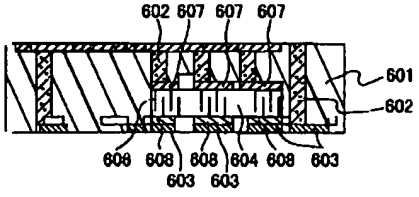

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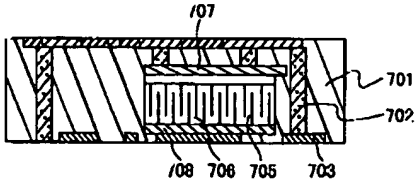

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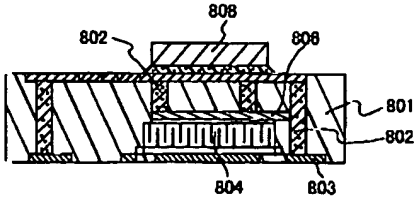

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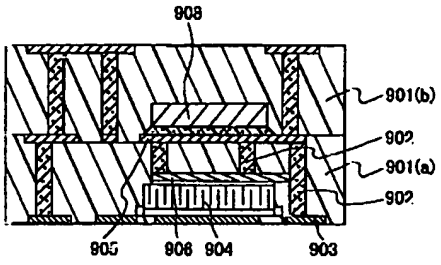

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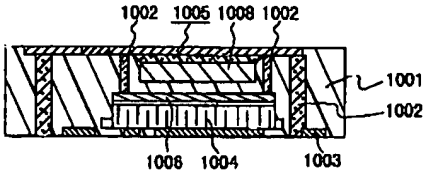

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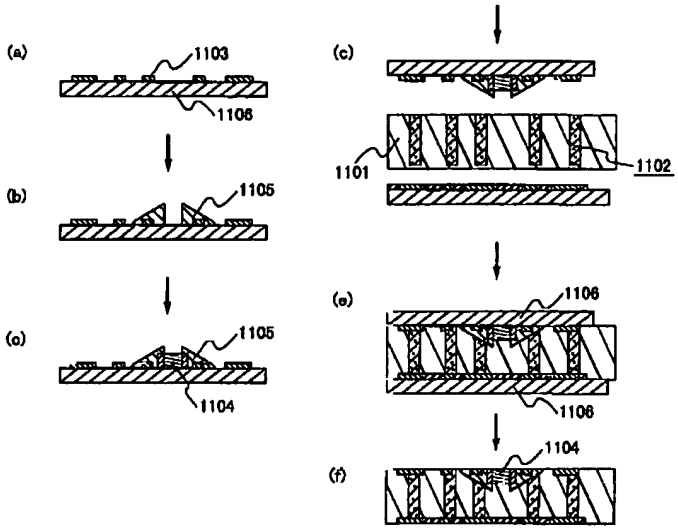

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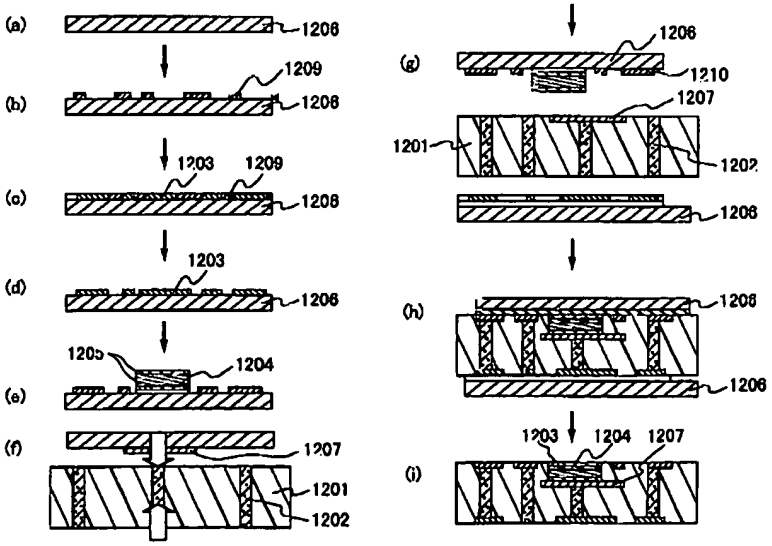

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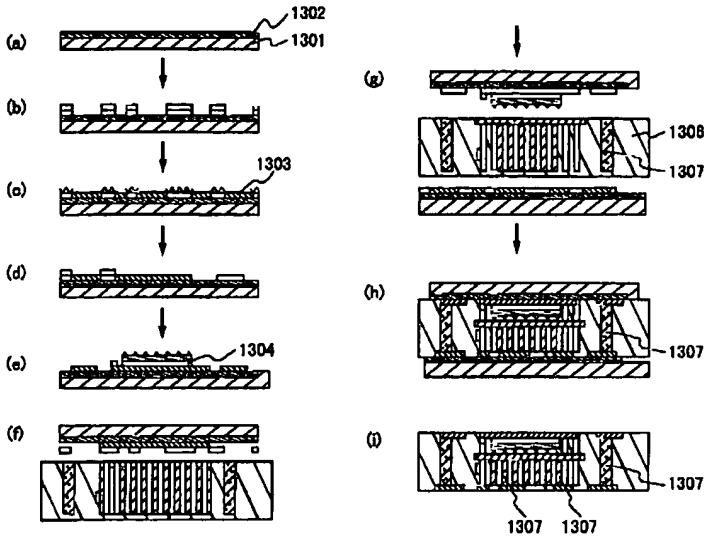
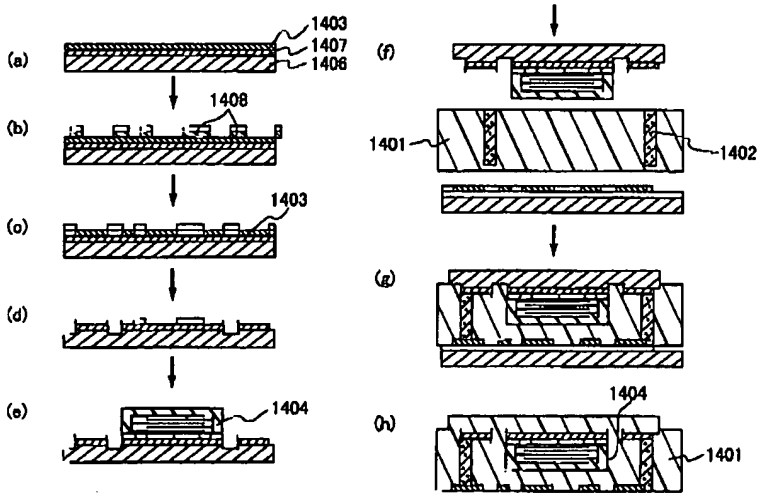
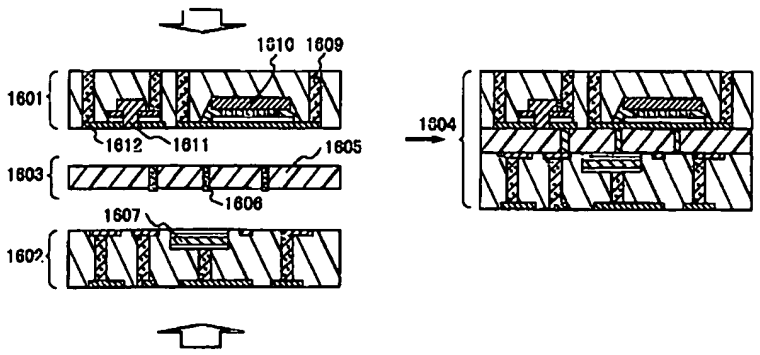

(a)
1302
1301
(b)
(c)
1303
(d)
(e)
1304
(f)
(g)
1308
1307
(h)
1307
(i)
1307
1307
1307

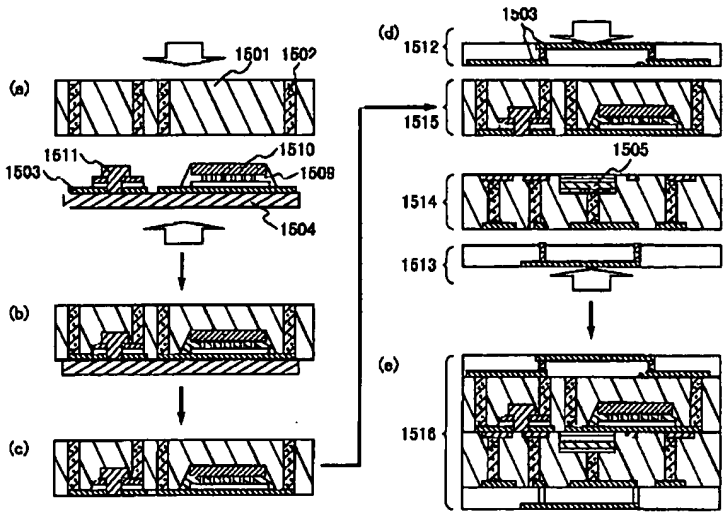
【図14】


(a)
1403
1407
1406
(b)
1408
(c)
1403
(d)
(e)
1404
(f)
1401
1402
(g)
(h)
1404
1401

【図16】


1610
1609
1601
1612
1611
1605
1603
1606
1607
1602
1604

【図15】



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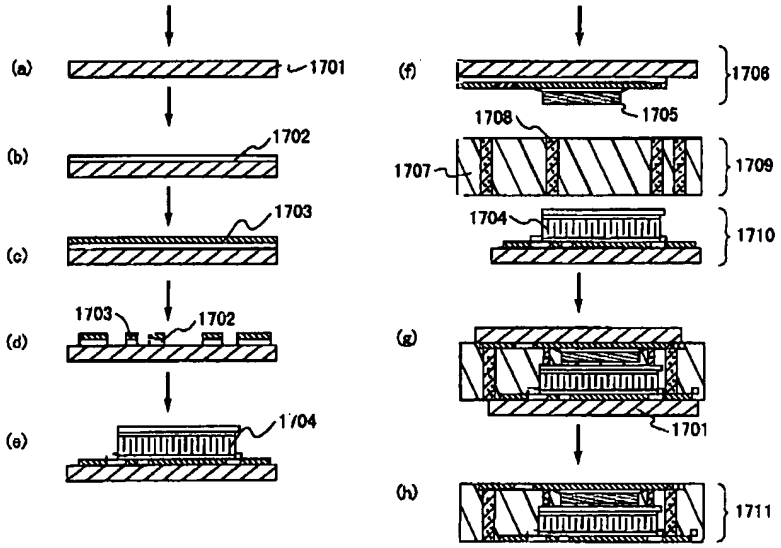

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